MARLON LESSING

ANALYSIS, DESIGN AND IMPLEMENTATION OF SINGLE-STAGE HIGH-FREQUENCY-ISOLATED DC-AC FLYBACK CONVERTERS



MARLON LESSING

ANALYSIS, DESIGN AND IMPLEMENTATION OF SINGLE-STAGE HIGH-FREQUENCY-ISOLATED DC-AC FLYBACK CONVERTERS



Editora chefe Prof^a Dr^a Antonella Carvalho de Oliveira Editora executiva Natalia Oliveira Assistente editorial Flávia Roberta Barão Bibliotecária Janaina Ramos 2023 by Atena Editora Projeto gráfico Copyright © Atena Editora Camila Alves de Cremo Copyright do texto © 2023 Os autores Luiza Alves Batista Copyright da edição © 2023 Atena Nataly Evilin Gayde Editora Imagens da capa Direitos para esta edição cedidos à Atena Editora pelos autores. iStock Edição de arte Open access publication by Atena Luiza Alves Batista Editora



Todo o conteúdo deste livro está licenciado sob uma Licença de Atribuição *Creative Commons*. Atribuição-Não-Comercial-NãoDerivativos 4.0 Internacional (CC BY-NC-ND 4.0).

O conteúdo do texto e seus dados em sua forma, correção e confiabilidade são de responsabilidade exclusiva do autor, inclusive não representam necessariamente a posição oficial da Atena Editora. Permitido o *download* da obra e o compartilhamento desde que sejam atribuídos créditos ao autor, mas sem a possibilidade de alterá-la de nenhuma forma ou utilizá-la para fins comerciais.

Todos os manuscritos foram previamente submetidos à avaliação cega pelos pares, membros do Conselho Editorial desta Editora, tendo sido aprovados para a publicação com base em critérios de neutralidade e imparcialidade acadêmica.

A Atena Editora é comprometida em garantir a integridade editorial em todas as etapas do processo de publicação, evitando plágio, dados ou resultados fraudulentos e impedindo que interesses financeiros comprometam os padrões éticos da publicação. Situações suspeitas de má conduta científica serão investigadas sob o mais alto padrão de rigor acadêmico e ético.

Conselho Editorial

Ciências Exatas e da Terra e Engenharias

Prof. Dr. Adélio Alcino Sampaio Castro Machado – Universidade do Porto Prof^a Dr^a Alana Maria Cerqueira de Oliveira – Instituto Federal do Acre Prof^a Dr^a Ana Grasielle Dionísio Corrêa – Universidade Presbiteriana Mackenzie Prof^a Dr^a Ana Paula Florêncio Aires – Universidade de Trás-os-Montes e Alto Douro Prof. Dr. Carlos Eduardo Sanches de Andrade – Universidade Federal de Goiás Prof^a Dr^a Carmen Lúcia Voigt – Universidade Norte do Paraná Prof. Dr. Cleiseano Emanuel da Silva Paniagua – Instituto Federal de Educação, Ciência e Tecnologia de Goiás Prof. Dr. Douglas Gonçalves da Silva – Universidade Estadual do Sudoeste da Bahia Prof. Dr. Eloi Rufato Junior – Universidade Tecnológica Federal do Paraná Prof^a Dr^a Érica de Melo Azevedo – Instituto Federal do Rio de Janeiro Prof. Dr. Fabrício Menezes Ramos – Instituto Federal do Pará Prof^a Dr^a Glécilla Colombelli de Souza Nunes – Universidade Estadual de Maringá Prof^a Dr^a Iara Margolis Ribeiro – Universidade Federal de Pernambuco Prof^a Dra. Jéssica Verger Nardeli – Universidade Estadual Paulista Júlio de Mesquita Filho

Prof. Dr. Juliano Bitencourt Campos – Universidade do Extremo Sul Catarinense Prof. Dr. Juliano Carlo Rufino de Freitas – Universidade Federal de Campina Grande Prof^a Dr^a Luciana do Nascimento Mendes – Instituto Federal de Educação, Ciência e Tecnologia do Rio Grande do Norte

Prof. Dr. Marcelo Marques - Universidade Estadual de Maringá

Prof. Dr. Marco Aurélio Kistemann Junior - Universidade Federal de Juiz de Fora

Prof^a Dr^a Maria José de Holanda Leite – Universidade Federal de Alagoas

Prof. Dr. Miguel Adriano Inácio - Instituto Nacional de Pesquisas Espaciais

Prof. Dr. Milson dos Santos Barbosa - Universidade Tiradentes

Prof^a Dr^a Natiéli Piovesan – Instituto Federal do Rio Grande do Norte

Prof^a Dr^a Neiva Maria de Almeida - Universidade Federal da Paraíba

Prof. Dr. Nilzo Ivo Ladwig - Universidade do Extremo Sul Catarinense

Prof^a Dr^a Priscila Tessmer Scaglioni – Universidade Federal de Pelotas

Prof^a Dr Ramiro Picoli Nippes – Universidade Estadual de Maringá

Prof^a Dr^a Regina Célia da Silva Barros Allil - Universidade Federal do Rio de Janeiro

Prof. Dr. Sidney Gonçalo de Lima - Universidade Federal do Piauí

Prof. Dr. Takeshy Tachizawa - Faculdade de Campo Limpo Paulista

Analysis, design and implementation of single-stage highfrequencyisolated DC-AC flyback converters

Diagramação:Camila Alves de CremoCorreção:Soellen de BrittoIndexação:Amanda Kelly da Costa VeigaRevisão:O autorAutor:Marlon Henrique Lessing

Dados Internacionais de Catalogação na Publicação (CIP)		
L639	Lessing, Marlon Henrique Analysis, design and implementation of single-stage highfrequency-isolated DC-AC flyback converters / Marlon Henrique Lessing. – Ponta Grossa - PR: Atena, 2023.	
	Formato: PDF Requisitos de sistema: Adobe Acrobat Reader Modo de acesso: World Wide Web Inclui bibliografia ISBN 978-65-258-1096-6 DOI: https://doi.org/10.22533/at.ed.966232404	
	1. Frequency converters. I. Lessing, Marlon Henrique. II. Título.	
	CDD 621.31	
Elaborado por Bibliotecária Janaina Ramos - CRB-8/9166		

Atena Editora Ponta Grossa – Paraná – Brasil Telefone: +55 (42) 3323-5493 www.atenaeditora.com.br contato@atenaeditora.com.br

DECLARAÇÃO DO AUTOR

O autor desta obra: 1. Atesta não possuir qualquer interesse comercial que constitua um conflito de interesses em relação ao conteúdo publicado; 2. Declara que participou ativamente da construção dos respectivos manuscritos, preferencialmente na: a) Concepção do estudo, e/ou aquisição de dados, e/ou análise e interpretação de dados; b) Elaboração do artigo ou revisão com vistas a tornar o material intelectualmente relevante; c) Aprovação final do manuscrito para submissão.; 3. Certifica que o texto publicado está completamente isento de dados e/ou resultados fraudulentos; 4. Confirma a citação e a referência correta de todos os dados e de interpretações de dados de outras pesquisas; 5. Reconhece ter informado todas as fontes de financiamento recebidas para a consecução da pesquisa; 6. Autoriza a edição da obra, que incluem os registros de ficha catalográfica, ISBN, DOI e demais indexadores, projeto visual e criação de capa, diagramação de miolo, assim como lançamento e divulgação da mesma conforme critérios da Atena Editora.

DECLARAÇÃO DA EDITORA

A Atena Editora declara, para os devidos fins de direito, que: 1. A presente publicação constitui apenas transferência temporária dos direitos autorais, direito sobre a publicação, inclusive não constitui responsabilidade solidária na criação dos manuscritos publicados, nos termos previstos na Lei sobre direitos autorais (Lei 9610/98), no art. 184 do Código Penal e no art. 927 do Código Civil; 2. Autoriza e incentiva os autores a assinarem contratos com repositórios institucionais, com fins exclusivos de divulgação da obra, desde que com o devido reconhecimento de autoria e edição e sem qualquer finalidade comercial; 3. Todos os e-book são *open access, desta forma* não os comercializa em seu site, sites parceiros, plataformas de *ecommerce*, ou qualquer outro meio virtual ou físico, portanto, está isenta de repasses de direitos autorais aos autores; 4. Todos os membros do conselho editorial são doutores e vinculados a instituições de ensino superior públicas, conforme recomendação da CAPES para obtenção do Qualis livro; 5. Não cede, comercializa ou autoriza a utilização dos nomes e e-mails dos autores, bem como nenhum outro dado dos mesmos, para qualquer finalidade que não o escopo da divulgação desta obra.

Document presented as a Thesis to obtain the degree of Master of Science in Electrical Engineering, of the Department of Electronics (DAELE), of the Federal University of Technology of Paraná.

Prof. Dr. Eloi Agostini Junior

I would first like to thank my dad for giving me the initial push to start this program and as the time went by for all the conversations, counsel, support and sympathetic ear.

I would like to thank my mom for supporting me all the way, whenever I needed.

To my better half Aline for supporting me, sharing my frustrations, my joys and tears.

I would like to express my deep gratitude to my advisor Prof. Dr. Eloi Agostini Jr. for his exceptional assistantship. I have learned a lot since I became Dr. Eloi's student. His door was always open whenever I ran into a trouble spot or had questions that I could not resolve on my own.

My sincere gratitude to Prof. Dr. Claudinor Bitencourt Nascimento for putting your trust in me and to Prof. Dr. Angelo Marcelo Tusset for giving me the initial push.

To my friends Gabriel de Oliveira Assunção, Gabriel R. Broday and William de Jesus Kremes for the technical discussions, friendly environment, friendship and solicitude.

To all my friends and relatives who had to deal with my absence.

To my teachers and colleagues.

To the Brazilian people who, through their hard work in difficult times, funded my formation.

SYMBOLS AND ABBREVIATIONS 1
ABSTRACT
RESUMO 5
INTRODUCTION
OBJECTIVES
STATE OF THE ART10
DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUTPUT CONNEC- TION
INTRODUCTION14
COMPLEMENTARY SWITCHING STRATEGY
Operating Stages for the Complementary Switching Strategy17
Static Analysis
Magnetizing Inductances ($L_{_{M1}}$ and $L_{_{M2}}$)
Output Capacitors (C_A and C_B)
Switch S _{IP} 25
Switch $S_{_{IN}}$
Switch <i>S</i> _{2P}
Switch <i>S</i> _{2N}
Small-signal Analysis for the Complementary Switching Strategy with Resistive Output Load
Small-signal Analysis for the Complementary Switching Strategy Coupled to an Output Voltage Source
ALTERNATIVE SWITCHING STRATEGY
Operating Stages for the Alternative Switching Strategy41
Static Analysis – Alternative Switching Strategy45
Magnetizing Inductances (L_{M1} and L_{M2})
Output Capacitors (C_A and C_B)
Switch <i>S</i> _{1P}

Switch <i>S</i> ₂ <i>p</i>
Switch <i>S</i> _{1N}
Switch <i>S</i> _{2N}
Small-signal Analysis for the Alternative Switching Strategy with Resistive Ou- tput Load
Small-signal Analysis for the Alternative Switching Strategy Coupled to an Output Voltage Source
CONCLUSION
DESIGN, SIMULATION AND EXPERIMENTAL RESULTS OF A DC-AC FLYBACK CONVERTER
INTRODUCTION
DESIGN METHODOLOGY60
REQUIREMENTS SPECIFICATIONS
NUMERICAL SIMULATION63
Complementary Switching Strategy64
Alternative Switching Strategy72
Comparison of Simulation Results
CHOICE OF COMPONENTS AND PROTOTYPE BUILT
Switches
Output Filter Capacitors
Flyback Inductor
Clamp Circuit
Prototype
EXPERIMENTAL RESULTS
Complementary Switching – Non-linearized Output
Complementary Switching – Linearized Output
Complementary Switching Strategy – Nonlinear Load
Alternative Switching Strategy – Non-linearized Output

Alternative Switching – Linearized Output	97
Alternative Switching Strategy – Nonlinear Load	100
Efficiency Tests	101
CONCLUSION	103
ACTIVE-CLAMPING SINGLE-STAGE FLYBACK CONVERTER.	105
INTRODUCTION	105
SWITCHING STRATEGY	108
OPERATING STAGES	108
STATIC ANALYSIS	112
AUXILIARY SWITCHING INDUCTOR (<i>LG</i>)	119
MAGNETIZING INDUCTANCE (<i>LM</i>)	121
AUXILIARY SWITCHING CAPACITOR (CG)	122
MAIN SWITCH (S1)	123
AUXILIARY ACTIVE-CLAMPING SWITCH (SG)	124
OUTPUT FILTER CAPACITOR (C_0)	125
BLOCKING DIODES (D_p AND D_N) AND SWITCHES (S_p AND S_N)	126
SMALL-SIGNAL ANALYSIS WITH RESISTIVE OUTPUT LOAD	128
CONCLUSION	135
DESIGN, SIMULATION AND EXPERIMENTAL RESULTS OF TH TIVE CLAMPING FLYBACK CONVERTER	
INTRODUCTION	136
DESIGN METHODOLOGY	136
REQUIREMENTS SPECIFICATIONS	137
NUMERICAL SIMULATION	138
CHOICE OF COMPONENTS AND PROTOTYPE BUILT	149
Switches and diodes	149
Output filter capacitors	151

Magnetics	152
Auxiliary switching capacitor	153
Clamp circuit	154
Prototype	155
EXPERIMENTAL RESULTS	.155
100 kHz – Linearized output	156
50 Khz - Linearized output	162
Efficiency tests	167
CONCLUSION	.170
GENERAL CONCLUSION	172
REFERENCES	174
APPENDIX A	177
APPENDIX A – CALCULATIONS FOR THE DC-AC FLYBACK CONVERTER W DIFFERENTIAL OUTPUT CONNECTION – COMPLEMENTARY SWITCH STRATEGY	ING
APPENDIX B	187
APPENDIX B – CALCULATIONS FOR THE DC-AC FLYBACK CONVERTER W DIFFERENTIAL OUTPUT CONNECTION – ALTERNATIVE SWITCHING STR GY	ATE-
APPENDIX C	195
APPENDIX C – CALCULATION OF LOSSES FOR THE DC-AC FLYBACK CON TER WITH DIFFERENTIAL OUTPUT CONNECTION – COMPLEMENTARY SY CHING	WIT-
APPENDIX D	200
APPENDIX D – DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUT CONNECTION - COUPLED INDUCTOR	
APPENDIX E	204
APPENDIX E – CALCULATION OF LOSSES FOR THE DC-AC FLYBACK C VERTER WITH DIFFERENTIAL OUTPUT CONNECTION – ALTERNATIVE SY CHING	WIT-
APPENDIX F	211

APPENDIX F – DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUTPUT CONNECTION – PCB LAYOUT
APPENDIX G
APPENDIX G – CALCULATIONS FOR THE ACTIVE-CLAMPING DC/AC FLYBACK CONVERTER – 100 kHz
APPENDIX H
APPENDIX H - CALCULATIONS FOR THE ACTIVE-CLAMPING DC/AC FLYBACK CONVERTER – 50 kHz
APPENDIX I
APPENDIX I - CALCULATION OF LOSSES FOR THE DC-AC ACTIVE- CLAMPING FLYBACK CONVERTER – COMPLEMENTARY SWITCHING 100 kHz235
APPENDIX J242
APPENDIX J - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER - COUPLED INDUCTOR 100 kHz
APPENDIX K
APPENDIX K - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER - COUPLED INDUCTOR 50 kHz
APPENDIX L
APPENDIX L - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER – AUXILIARY SWITCHING INDUCTOR 100 kHz
APPENDIX M255
APPENDIX M - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER – AUXILIARY SWITCHING INDUCTOR 50 kHz
APPENDIX N
APPENDIX N - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER – PCB LAYOUT

SYMBOLS AND ABBREVIATIONS

Symbol – description [units]

α	Angle for the ac variations	
∆t,	Duration of the first operating stage [s]	
$\Delta \hat{t}_{1}(s)$	Linearized duration of the first operating stage [s]	
∆t3	Duration of the third operating stage [s]	
$\Delta \hat{t}_{3}(s)$	Linearized duration of the third operating stage [s]	
∆t₄	Duration of the fourth operating stage [s]	
$\Delta t_{4}(s)$	Linearized duration of the fourth operating stage [s]	
Δt_{6}	Duration of the sixth operating stage [s]	
$\Delta t_{6}^{"}(s)$	Linearized duration of the sixth operating stage [s]	
Δt_{7}	Duration of the seventh operating stage [s]	
$\Delta \hat{t}_{7}(s)$	Linearized duration of the seventh operating stage [s]	
ΔV_{o}	Output voltage ripple [V]	
$\Delta V_{0\%}$	Percentage of the output voltage for ripple calc.	
ΔI_{LM}	Current ripple in the magnetizing inductance [A]	
$\Delta I_{LM\%}$	Percentage of the current in the magnetizing inductance for ripple calc.	
C_o	Output capacitor [F]	
C_1	S1 intrinsic capacitor [F]	
$C_{_{G}}$	Auxiliary switching capacitor [F]	
C_{sG}	SG intrinsic capacitor [F]	
D	Duty cycle	
D'	(1-D) duty cycle	
d	Variable duty cycle	
d(t)	Duty cycle variable in the time domain	
<i>d</i> (<i>s</i>)	Duty cycle variable in the frequency domain	
D _{max}	Duty cycle for maximum power output	
D ₁	S1 anti-parallel diode	
D_N	Blocking diode	
D_P	Blocking diode	
D_{sG}	SG anti-parallel diode	
f _s	Switching frequency [Hz]	
I_0 $\hat{i}_0(t)$	Output current [A]	
$i_{0}(t)$	Output current variable in time domain [A]	
î ₀ (s)	Output current variable in frequency domain [A]	
Ι,	Current in the magnetizing inductance – start 1 st stage [A]	
I_2	Current in the magnetizing inductance – start 3 rd stage [A]	
I_A	Current in the capacitor $C_{A}[A]$	
I _B	Current in the capacitor $C_{B}[A]$	
I,	Current in the inductor L_o [A]	
$\hat{i}_{L0}(t)$	I_{LO} variable in time domain [A]	
í _{L0} (s)	ILO variable in frequency domain [A]	

 $I_{I,M1}$ Current in the mag. inductance L_{M} [A] i , M1 (t) I, M1 variable in time domain [A] i _{LM1} (s) I_{IM} variable in frequency domain [A] Current in the mag. inductance L_{M2} [A] I_{M2} I_{IM2} variable in time domain [A] $i_{1M2}(t)$ i _{LM2} (s) I, M2 variable in frequency domain [A] Current in the mag. inductance - starts 6th stage [A] I_{LX} Current in the switch S_{1} [A] I_{S1} $I_{S^{1N}}$ Current in the switch S_{1N} [A] Maximum current in S_{1N} [A] I_{S1Nmax} Maximum current in S_{IN} [A] I_{S1Nmin} Current in the switch S_{η_P} [A] I_{S1P} Maximum current in S_{IP} [A] I_{S1Pmax} Minimum current in S_{1P} [A] I_{S1Pmin} Current in the switch S_{N} [A] I Current in the switch S_{P} [A] ISP Current in the switch S_{2p} [A] I_{S2P} Maximum current in S_{PP} [A] I S2Pmax Minimum current in S_{2P} [A] I_{S2Pmin} $i_{SPP}(t)$ I_{sop} variable in time domain [A] I_{S2P} variable in frequency domain [A] i _{sop} (s) Current in the switch S_{2N} [A] I_{S2N} Maximum current in S_{2N} [A] I_{S2Nmax} Minimum current in S_{2N} [A] I S2Nmin $i_{S2N}(t)$ I_{S2N} variable in time domain [A] i _{sen} (s) I_{S2N} variable in frequency domain [A] Choke inductor for grid connection [H] L L_{a} Auxiliary switching inductor [H] Magnetizing inductance [H] L_{M} Magnetizing inductance in the flyback inductor T1 [H] L_{M1} Magnetizing inductance in the flyback inductor T2 [H] L_{M2} М Static gain Turns ratio of the flyback transformer п P_{o} Output power Voltage conversion ratio q S_{1} Main switch of the dc-ac active-clamping flyback converter S_{1N} Switch in the primary winding of the flyback inductor T2 $S_{_{1P}}$ Switch in the primary winding of the flyback inductor T1 S_{2N} Switch in the secondary winding of the flyback inductor T2 Switch in the secondary winding of the flyback inductor T1 $S_{_{2P}}$ S_{G} Auxiliary switch of the dc-ac active-clamping flyback converter Switch in the secondary winding for the negative semi-cycle $S_{\scriptscriptstyle N}$ Switch in the secondary winding for the positive semi-cycle S_{P} Τ, Flyback Inductor

T_{2}	Flyback Inductor	
THD	Total harmonic distortion	
Ts	Switching period [s]	
V _o	Output Voltage [V]	
V ₀	Variable output voltage [V]	
$egin{aligned} & v_{_{0}} \ \hat{v}_{_{0}} \ (t) \ \hat{v}_{_{0}} \ (s) \end{aligned}$	Variable output voltage in time domain [V]	
$\hat{v}_{0}(s)$	Variable output voltage in frequency domain [V]	
V_{A}	Voltage on the capacitor CA [V]	
	Variable V_A voltage [V]	
\hat{v}_{A} \hat{v}_{A} (t)	Variable V_{A} in time domain [V]	
$\hat{v}_{A}(s)$	Variable V_A in frequency domain [V]	
$V_{\scriptscriptstyle B}$	Voltage on the capacitor CB [V]	
V _B	Variable V_{B} voltage [V]	
$\hat{v}_{B}(t)$	Variable V_{B} in time domain [V]	
$\hat{v}_{B}(s)$	Variable V_{B} in frequency domain [V]	
$V_{_{G}}$	Grid voltage [V]	
V_{G} $\hat{v}_{G}(t)$	Variable V_{G} in time domain [V]	
$\hat{v}_{_G}(s)$	Variable V_{G} in frequency domain [V]	
$V_{_{IN}}$	Input voltage [V]	
$\hat{v}_{_{IN}}(t)$	Variable input voltage in time domain [V]	
$\hat{v}_{_{IN}}(s)$	Variable input voltage in frequency domain [V]	
V_{L1}	Voltage across the magnetizing inductance L1 $\left[V \right]$	
V_{L2}	Voltage across the magnetizing inductance L2 [V]	
$V_{_{pk_pos}}$	Positive peak output voltage [V]	
ZVS	Zero voltage switching	

ABSTRACT

This thesis proposes the analysis of two single-stage high-frequency- isolated converters suited for grid-tied applications. Firstly, a new modulation strategy to the bidirectional flyback converter with differential output connection is introduced. This improved modulation provides better performance by reducing the RMS current values for every circuit element, thereby contributing to reduced conduction losses. The static analyses of the converter operating in both the original and the alternative switching strategies are presented. Dynamic analysis is also performed, providing the output-current-to-duty-cycle transfer function of the converter connected to a resistive load and coupled to an output voltage source. A 500 W, 20 kHz, 70 V input voltage and 127 V_{RMS} output voltage prototype is presented and experimental results comparing the new modulation strategy to the original confirm the theoretical analyses and superior performance of the alternative switching strategy. A low THD output voltage is achieved for both switching strategies, operating in open loop and in continuous conduction mode. The second converter is an active-clamping flyback converter suitable to be used as a microinverter in renewable energy applications. The main features of the topology are the relatively low component count, high-frequency isolation, voltage step-up capability and zero voltage switching. The active clamping allows to recover most of the energy stored in the flyback inductors' leakage inductance and thus an improvement on the system efficiency is achieved. The static analysis for CCM operation is provided. In addition, an output-currentto-duty-cycle transfer function for a resistive load connected to the output of the converter is presented. Two switching frequencies of 100 kHz and 50 kHz were tested in a prototype built for 500 W, 70 V input voltage and 127 V_{RMS} output voltage.

KEYWORDS: Flyback converter. Soft-switching. Single-stage. Differential output connection. High-frequency-isolated.

RESUMO

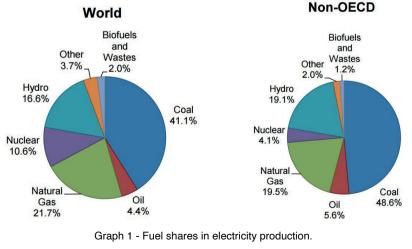
Esta dissertação propõe a análise de dois conversores de estágio único, isolados em alta frequência e adequados para aplicações de conexão à rede elétrica. Inicialmente, é introduzida uma nova estratégia de modulação para o conversor flyback bidirecional com conexão diferencial. Esta modulação melhorada proporciona melhor desempenho, reduzindo os valores de corrente RMS para cada componente do circuito, contribuindo assim para a redução das perdas por condução. As análises estáticas do conversor operando em ambas estratégias de modulação alternativa e original são apresentadas. A análise dinâmica também é realizada, fornecendo a funcão de transferência da corrente de saída pela razão cíclica do conversor ligado à uma carga resistiva e acoplado a uma fonte de tensão. Um protótipo com potência de saída de 500 W, 20 kHz, com tensão de entrada de 70 V e 127 $V_{\rm PMS}$ na tensão de saída é apresentado e os resultados experimentais que comparam a nova estratégia de modulação confirmam a análise teórica e desempenho superior. Uma tensão de saída com baixa THD é alcancada para ambas estratégias de modulação, operando em malha aberta em no modo de condução contínua. O segundo conversor é um flyback com grampeamento ativo adeguado para ser utilizado como um micro-inversor em aplicações de energias renováveis. As principais características da topologia são o relativo baixo número de componentes, o isolamento em alta frequência, possibilidade de ser utilizado como elevador de tensão de saída e operação em ZVS. O grampeamento ativo permite recuperar a maior parte da energia armazenada na indutância de dispersão dos indutores flyback e, assim, uma melhoria na eficiência do conversor é atingida. A análise estática é fornecida para o conversor operando em CCM. Além disso, uma função de transferência da corrente de saída pela razão cíclica é apresentada para uma carga resistiva na saída. Para este conversor duas frequências de comutação de 100 kHz e 50 kHz foram testadas num protótipo construído para 500 W, com tensão de entrada de 70 V e tensão de saída de 127 V_{pme}.

PALAVRAS-CHAVE: Conversor flyback. Comutação suave. Estágio único. Conexão diferencial. Isolação em alta frequência.

INTRODUCTION

In recent years, growing concerns for the environment along with the present legislation have increased the attention to renewable energy sources. With the constant economy growth and development of the industry, the demand for sustainable energy has been a recurring theme. In this context, the industry and society, heavily dependent on the energy yielded from sources like oil, gas, coal, hydropower and biomass, has its best choice in the renewable energy sources for its future progress.

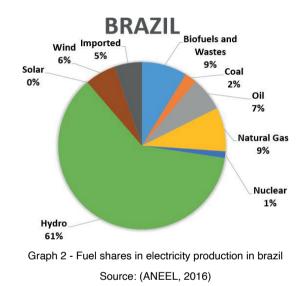
According to (IEA STATISTICS, 2016), in 2013, 67.2% of the global electricity production was from fossil fuel-power plants. Hydroelectric plants provided 16.6%, nuclear plants 10.6%, biofuels and waste a total of 2%, while geothermal, solar, wind and other sources made up the remainder 3.6%. In 2014, electricity production in OECD (Organization for Economic Co-operation and Development) countries fell by 0.8%, mainly the result of a decrease in the usage of fossil fuels for electricity production. On the other hand, electricity generation from wind (8.1%), nuclear (0.9%) and solar (26.9%) increased in the same period. For the countries that are not members of the OECD, which includes Brazil, there are still incomplete information on the energy production in 2014, though in 2013 the gross electricity production increased 5.4% from 2012. In 2013, as presented in Graph 1, 73.8% of the non-OECD electricity production was generated from fossil fuels, 19% from hydroelectric plants, 4.1% by nuclear plants and 3.1% by biofuels, waste, geothermal/solar, and wind capacity.



Source: (IEA STATISTICS, 2016)

In Brazil, current data (Graph 2) show that 61.1% of the electricity production is generated from hydroelectric plants, 17.4% from fossil fuels, 8.7% from biomass and

wastes, 6% from wind and 1% by nuclear plants (ANEEL, 2016). Considering that 5.3% of the electricity consumed is imported from countries like Paraguay, Argentina, Venezuela and Uruguay, countries that have as its primary energy source hydropower, only 0.01% of the electricity available in Brazil is generated from solar capacity (ANEEL, 2016). The perspective, on the other hand, is encouraging. Of all the energy plants under construction, 33.8% correspond to wind power plants. According to the national governing body of electrical energy (ANEEL), the number of homes that generate electricity connected to the utility grid have risen from 424 connections in 2014 to 1731 in 2015 with power capacity of 16.565 kW, being 96.7% from solar power (CIASOLAR). In addition, ANEEL states that an increase of 800% of connections is expected for the current year of 2016 in comparison to 2015.

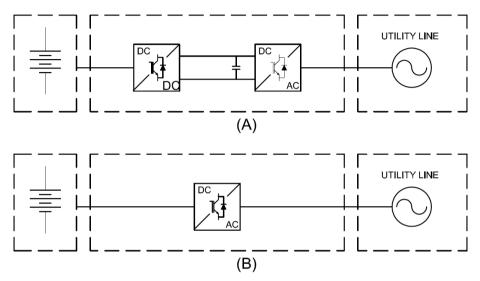


Although the electricity production from renewables like wind and solar energy around the world are still diminutive in comparison to other sources, the International Energy Agency (IEA) states that these two are currently the fastest-growing sources of electricity globally (IEA, 2016).

Electricity is generated from the solar energy converting the radiation into electricity in photovoltaic (PV) systems. A PV system employs solar panels to supply electricity, which are connected to the power grid by means of an inverter that converts the panel's DC output power into AC power. Likewise, wind power is converted into electricity using wind turbines. In a similar way, the photovoltaic systems and the wind turbines are better integrated to the power grid using power electronics to meet the requirements of the electric grid.

In Brazil, for photovoltaic systems below 10 kW, the INMETRO #17 decree of January 14th, 2016 states that grid-tied inverters are not required to have galvanic isolation from the

input to the output. Similarly, the technical norm NTC 905200 from the power distribution company in the Paraná state (COPEL) states that inverters that perform the connection of a generator to the utility line does not require galvanic isolation for the same power range of 10 kW. The non-isolated system configuration, concerning its connection to the utility grid, can be performed in a single stage or in two stages, considering a dc power source, as in Figure 1.



 $\label{eq:Figure 1-(A) Two-stage configuration. (B) Single-stage configuration.} \\ Source: Self-authorship$

However, for isolated configurations, considering a dc power source, the system configuration may vary from multiple stages to a single stage, as depicted in Figure 2. The most simplistic way to connect a DC voltage source to the power grid using power electronics is a system that connects a DC link step-up converter to a DC- AC inverter isolated by a low frequency transformer at its output, as Figure 2 (A) shows. The main advantages of this system are the robustness and the low cost of implementation. However, in systems where higher efficiency is required, better configurations that does not require a low frequency transformer are preferred. In this case, either of the converters can provide galvanic isolated DC-DC step-up converter or a high-frequency isolated DC-AC inverter replaces its respective counterpart. Figure 2 (B) shows a system that operates with a high-frequency isolated DC-DC step-up converter. Ultimately, in order to increase the levels of efficiency and to meet the requirements of reduced cost and volume, the energy conversion can be performed in a single stage. This configuration consists of a DC-AC inverter that

8

connects the DC source to the utility grid, as shown in Figure 2 (C).

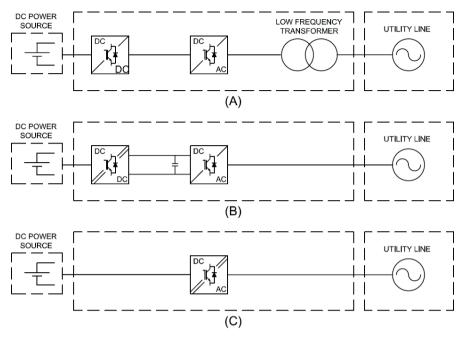


Figure 2 - (A) Two-stage low-frequency-isolated configuration. (B) Two-stage high-frequency-isolated configuration. (C) Single-stage high-frequency-isolated configuration.

Source: Self-authorship

1 | OBJECTIVES

Although not required for the range of the application, the objectives of this work are to study, design and implement single-stage high-frequency isolated micro- inverters suited for grid connection of renewable energy sources. Thereby, the rated output power of the inverters studied and implemented are below 1 kW, which means that galvanic isolation is not required by any of the current standards in Brazil. However, considering that the inverters proposed in this study are based on the flyback topology, therefore an isolated version of the buck-boost converter, the coupled inductor can benefit the design of the converter by means of the turns ratio, which can be used to bolster the efficiency levels of the converter.

Because the output voltage of most photovoltaic panels varies from 6 to 24 V, the voltage step-up required for a buck-boost inverter in a 127 VRMS grid connection would depend heavily on the duty cycle of the converter to reach certain static gain. For a 220 VRMS grid connection, the problem becomes even more pronounced. On the other hand, when the dc power source is a small wind turbine, the voltage levels are usually higher and the problem can be minimized. Therefore, the turns ratio of the flyback inductor can help

reach higher static gains without degrading the efficiency of the converter.

21 STATE OF THE ART

The most common way to obtain a sinusoidal output from a converter is to use either a two-level sinusoidal pulse width modulation (SPWM) or a three-level PWM in a full bridge converter. According to (CARDOSO, 2007), the main disadvantage of the configuration presented in Figure 3, is that this topology cannot be isolated in high frequency due to the asymmetric relation of the switching frequency and the waveform of the voltage in the primary of the transformer.

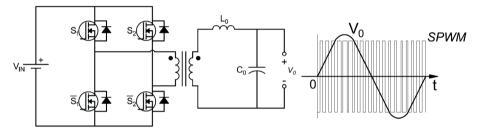


Figure 3 - Low-frequency-isolated full bridge inverter. Source: Self-authorship

The solution for this problem is to use the converter in order to generate a high-frequency-isolated ac bus, as previously shown in Figure 2 (B) and (C).

Regarding renewable energy applications, usually researchers have explored the two-stage solution as a boost type converter to step-up the voltage to a higher value for the first stage and a full-bridge converter for the second stage to inject current to the grid, using a low frequency transformer for grid connection, as in (CAO, MA, *et al.*, 2013), (JAIN e SINGH, 2014) and Figure 4. Others have used a low-frequency- isolated full-bridge connected to a buck converter that does not require an additional transformer for grid connection, as in (CHEN, AMIRAHMADI, *et al.*, 2013). Figure 5 presents a single-phase version of the converter presented in (CHEN, AMIRAHMADI, *et al.*, 2013).

The two-stage configuration in Figure 4 can also be achieved by using different topologies for either DC link step-up, such as the Cùk converter proposed in (SYAM e KAILAS, 2013) and the boost type converters proposed in (MAROUANI, ECHAIEB e MAMI, 2012) and (MARIKKANNAN, MANIKANDAN e JAYANTHI, 2014). The possibilities for the two-stage configuration are countless for either the first stage or the second stage where the combination of different topologies will give different results.

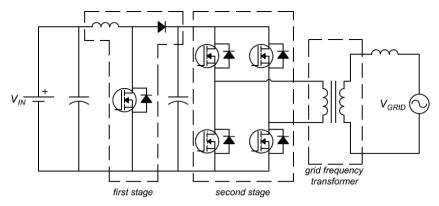


Figure 4 - Conventional two-stage configuration.

Source: Self-authorship

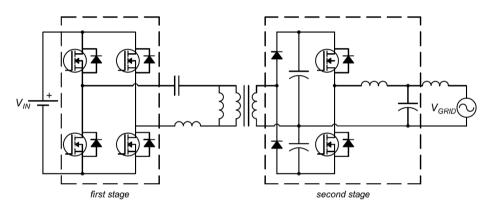


Figure 5 – Single-phase two-stage configuration Source: Self-authorship

It is in the single-stage configuration that lower component count, increased reliability and overall higher efficiency levels are observed. Although the DC-AC boost converter presented by (CACERES e BARBI, 1999) in Figure 6 is not isolated, the low component count, simplicity, low harmonic distortion and the possibility of operating as bidirectional converter makes this an attractive design for uninterruptible power supply (UPS) systems.

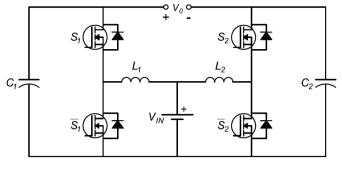


Figure 6 - Boost DC-AC converter Source: Self-authorship

In (HU, CHANG e XUE, 2008) two non-isolated buck-boost converters intended for the connection of small wind turbine to the utility grid are presented. Whilst there are no isolation between the input and output voltage, the low component count, most directed to the switching devices, leads to low cost and potentially higher efficiency levels.

It is observed that both converters in Figure 7 have coupled inductors in its circuits, which can also be used as a flyback inductor in order to provide galvanic isolation between input and output, as presented by (CIMADOR e PRESTIFILIPPO, 1990) and shown in Figure 8. In this converter, the requirements of low component count, possibility of operating as a boost converter and low harmonic distortion are satisfied, as well as the galvanic isolation, absent in the converters presented in Figure 6 and Figure 7 (A) and (B).

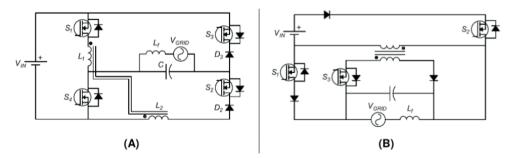


Figure 7 - Single-stage buck-boost converter. (A) 4 switches. (B) 3 switches. Source: Self-authorship

Furthermore, the single-stage configuration benefits the flyback converter as a DC-AC inverter because of its simplicity, low component count, reliability and low harmonic distortion in most cases observed. Figure 9 shows a flyback inverter presented in (KASA, IIDA e CHEN, 2005), in which all the discussed advantages of the flyback converter are observed for a single-stage grid connection.

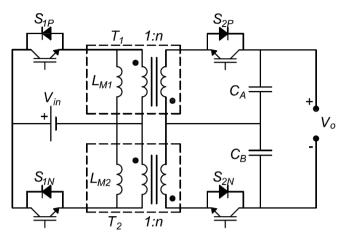


Figure 8 - DC-AC flyback converter with differential output connection.

Source: Self-authorship

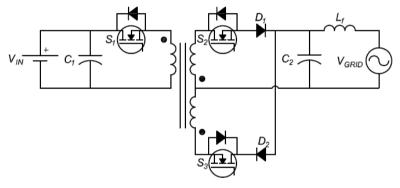


Figure 9 - DC-AC flyback inverter. Source: Self-authorship

This research aims to study two topologies of converters for the single-stage high-frequency-isolated configuration presented in Figure 2 (C). Chapter 2 presents two modulation strategies for the high-frequency-isolated DC-AC flyback converter with differential output connection previously shown in Figure 8. Simulation and experimental results for both modulation strategies for this topology are presented in Chapter 3. An intermediate discussion of the results presented in Chapter 3 are presented in Chapter 4 as well as a new active-clamping circuit for the converter shown in Figure 9. Chapter 5 exhibit the simulation and experimental results for the study hereon.

DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUTPUT CONNECTION

The flyback converter is a well-known example of isolated converter, which can be used as a single-stage converter for grid application. This chapter presents the topology proposed by (CIMADOR e PRESTIFILIPPO, 1990), its operating stages for the original switching strategy, voltage conversion ratio, dynamic behavior and the efforts in all elements in the circuit. Next, an alternative switching strategy that aims to reduce the current stress and voltage levels in all switching devices in the circuit is proposed. Both converters are studied operating in continuous conduction mode (CCM).

1 | INTRODUCTION

The original DC-DC flyback converter is derived from the buck-boost converter. However, as an advantage the flyback inductor offers galvanic isolation that the buckboost converter does not have. In addition, the turns ratio of the flyback inductor offers an additional degree of freedom in relation to the static characteristics of the converter, which means that the voltage conversion ratio is not solely dependable on the duty cycle.

The differential connection of two DC-DC bidirectional converters switching at high frequency allows to create a bidirectional DC-AC isolated converter (CIMADOR e PRESTIFILIPPO, 1990). By this definition, these converters produce a DC biased sine wave output, so that each converter produces a unipolar voltage. The topology of the converter proposed by (CIMADOR e PRESTIFILIPPO, 1990) is shown in Figure 10. This converter is originally switched using the complementary switching modulation, whereupon switches S_{1P} and S_{2N} receive the same command as well as switches S_{1N} and S_{2P} regardless of the output. That is, assuming that S_{1P} and S_{2N} remains on in DTs seconds, S_{1N} and S_{2P} will conduct during an interval of $(1 - D)T_s$ seconds.

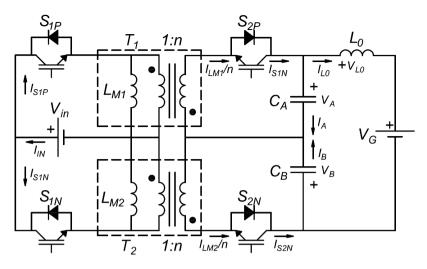


Figure 10 - Bidirectional DC-AC flyback converter with differential output. Source: self-authorship

In (SKINNER, 1993), the author proposes a simplification of the model presented by (CIMADOR e PRESTIFILIPPO, 1990), as Figure 11 shows. This converter presents an interesting modulation strategy in which one of the switches in the secondary of the flyback inductor has to remain turned on for a whole semi-cycle of the AC output while its counterpart in the primary winding of the flyback inductor remains blocked. Meanwhile, the other two switches are commanded with complementary pulses. In other words, while one conducts during DT_s seconds the other remains on in $(1-D)T_s$ seconds, as Figure 12 (B) shows. This modulation strategy allows reducing the switching losses in the secondary as well as reducing the RMS value of the current in each one of the switches. Figure 12 (A) presents the switching strategy for the converter of Figure 10, while Figure 12 (B) presents the switching strategy for the converter shown in Figure 11.

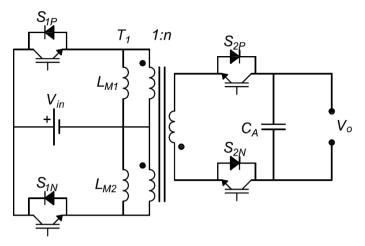


Figure 11 - Bidirectional DC-AC flyback converter proposed in (SKINNER, 1993). Source: self-authorship

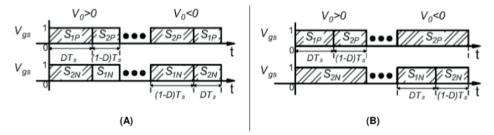


Figure 12 - Modulation strategies. (A) Complementary switching strategy proposed by (CIMADOR e PRESTIFILIPPO, 1990). (B) Switching strategy proposed by (SKINNER, 1993).

Source: self-authorship

This chapter studies the operation of both modulation strategies shown in Figure 12 for the converter presented by (CIMADOR e PRESTIFILIPPO, 1990) and shown in Figure 10.

2 | COMPLEMENTARY SWITCHING STRATEGY

The circuit of the DC-AC flyback converter with differential output connection consists of two switches located in the primary of the flyback inductor: S_{1P} and S_{1N} ; two flyback inductors (T_1 and T_2) with their magnetizing inductances (L_{M1} and L_{M2} , respectively) and turns ratio of 1:n. In the secondary windings of both flyback inductors there are two bidirectional switches: S_{2P} and S_{2N} ; and two output capacitors *CA* and *CB* acting as output filters.

The complementary switching strategy in this converter, consists in switching $S_{_{1P}}$ and $S_{_{2N}}$ in DT_s seconds and both $S_{_{2P}}$ and $S_{_{1N}}$ in $(1-D)T_s$, where D represents the duty cycle of the converter and T_s is the switching period. However, to generate an alternate output the PWM

carrier is compared to a sine wave that varies from 0 to 1 with its origin placed in 0.5. The output of the converter is positive when *D*>0.5, which means that the angular variation (*a*) of the sine wave varies from 0 to p. Similarly, the output is negative when *D*<0.5, meaning that $\pi < a < 2\pi$. Figure 13 presents the desired output voltage response of the converter operating under the complementary switching strategy.

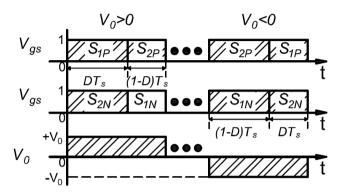
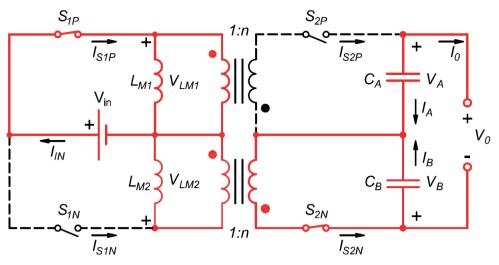


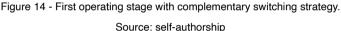
Figure 13 – Switching signals and output voltage for the complementary switching strategy. Source: self-authorship

2.1 Operating Stages for the Complementary Switching Strategy

To simplify the analysis, all semiconductors are considered ideal; the flyback inductors are modeled as an ideal transformer with their magnetizing inductances L_{M1} and L_{M2} . The turns ratio is defined from the primary to the secondary winding, which reads 1:*n*. The turns ratio is equal to *n* and is the same for both inductors.

Figure 14 shows the equivalent circuit of the converter during the first operating stage. The dashed lines represent the absence of current in that circuit branch.





In the first operating stage, S_{1P} turns on, charging the magnetizing inductance L_{MI} . Considering that S_{1P} and S_{2N} turn on at the same time (see Figure 13), the magnetizing inductance L_{M2} transfers energy to the secondary and to the output of the converter. The output current in this stage circulates through the capacitor C_A , which is connected in series with the output load, while C_B charges. In this operating stage, S_{2P} and S_{1N} are blocked.

In the second operating stage of the converter, switch $S_{_{1P}}$ is turned off, and the energy in $L_{_{M1}}$ is transferred to the secondary as $S_{_{2P}}$ turns on. Switch $S_{_{1N}}$ turns on to charge the magnetizing inductance $L_{_{M2}}$ and $S_{_{2N}}$ is turned off. In this operating stage, the output current passes through the capacitor $C_{_B}$ while $C_{_A}$ charges. Figure 15 shows the equivalent circuit of the converter during the second operating stage.

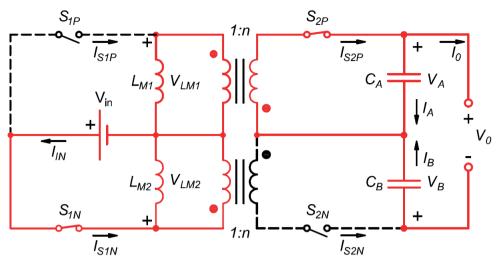


Figure 15 - Second operating stage with complementary switching strategy Source: self-authorship

In summary, the complementary modulation strategy corresponds to the condition where the duty cycles of the two flyback modules are complementary to each other. For example, if the upper flyback module is driven by a duty cycle *D*, the lower by (1-*D*), and vice-versa.

It is noteworthy that the implementation of this switching strategy is only possible if there is a dead time between the operating stages of the converter, so there is no overlap of the control pulses to the switches, which causes short circuit between the primary and secondary windings of the flyback inductor. However, neither the dead time nor the impact it possibly has on the converter are considered for the analysis of the operating stages.

Based on the analysis of the two operating stages and the theoretical waveforms presented in Figure 16 and Figure 17, the voltages on the magnetizing inductances L_{MI} and L_{M2} and the currents through the capacitors C_A and C_B can be determined as presented in Table 1.

1 st Power Stage	2 nd Power Stage
$V_{L1} = V_{IN}$	$V_{L1} = -V_A/_n$
$V_{L2} = -V_B/n$	$V_{L2} = V_{IN}$
$I_{CA} = I_{S2P} - I_o$	$I_{CA} = -I_o$
$I_{CB} = -I_o$	$I_{CB} = I_{S2N} - I_o$

Table 1 – Inductors current and capacitors currents for CCM operation – complementary modulation strategy.

Source: Self-authorship

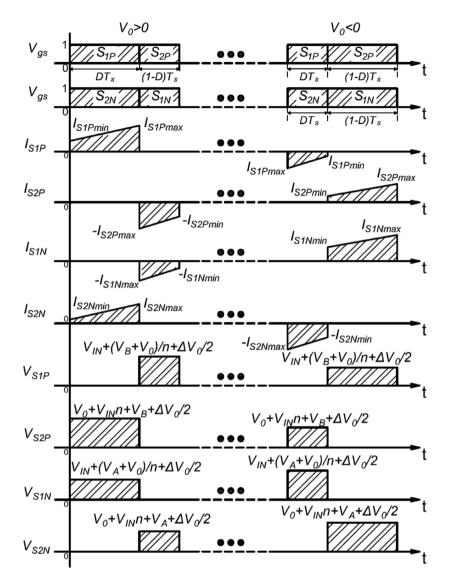


Figure 16 – Theoretical waveforms for CCM operation – complementary switching strategy – currents and voltages on the switches.

Source: self-authorship

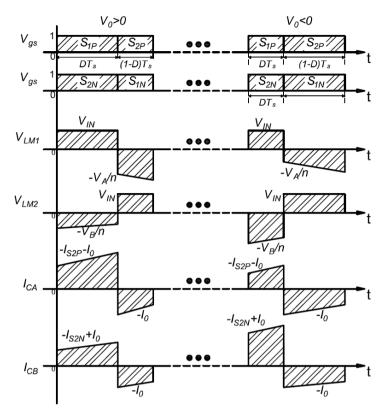


Figure 17 – Theoretical waveforms for CCM operation – complementary switching strategy – voltages on $L_{_{M1}}/L_{_{M2}}$ and Currents in $C_{_{A}}/C_{_{B}}$.

Source: self-authorship

2.2 Static Analysis

Using the principle of the volt-second balance in both magnetizing inductances $L_{_{M1}}$ and $L_{_{M2}}$ and the values provided in Table 1, it is possible to obtain the equations of the voltages $V_{_{A}}$ and $V_{_{B}}$, as given by (2.1) and (2.2), respectively.

$$V_A = \frac{nD}{1-D} \tag{2.1}$$

$$V_B = \frac{n(1-D)}{D} \tag{2.2}$$

From the analysis of the circuit presented in Figure 10, it is possible to verify that $V_0 = V_A - V_B$. The static gain *q* is defined as the ratio between the output voltage V_o and the input voltage V_{INP} as presented in (2.3).

$$q = \frac{V_0}{nV_{IN}} = \frac{2D - 1}{D(1 - D)}$$
(2.3)

Isolating D in (2.3) results in (2.4), which provides the duty cycle value that ensures the operation with a given static gain q.

$$D = \frac{q - 2n + \sqrt{q^2 + 4n^2}}{2q}$$
(2.4)

It is desired that the output voltage behaves as a sine function, where Vp refers to the peak value of the output voltage, as given by (2.5).

$$V_o(\alpha) = V_p \sin(\alpha) \tag{2.5}$$

Considering that a sinusoidal voltage is expected at the output of the converter, the duty cycle D for any given angle of the output voltage is obtained by replacing the definition (2.5) into the duty cycle equation (2.4), as shown in (2.6).

$$D(\alpha) = \frac{1}{2} \frac{V_{IN}}{V_p \sin(\alpha)} \left(\frac{V_p \sin(\alpha)}{V_{IN}} - 2 + \sqrt{\frac{V_p \sin(\alpha)}{V_{IN}}} + 4 \right)$$
(2.6)

It is noteworthy that the same sinusoidal behavior is expected at the output current. Figure 18 presents the resulting curve of the duty cycle as the voltage conversion

ratio increases, given by equation (2.4).

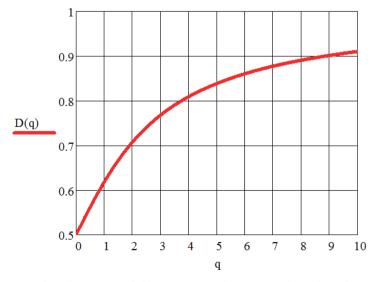


Figure 18 - Complementary switching strategy - voltage conversion ratio vs duty cycle. Source: Self-authorship

Similarly, a modulation index M can be defined as the relation of the output voltage by the input voltage, leaving the turns ratio of the flyback inductor as a separate constant of the voltage conversion ratio defined in (2.3), as presented in (2.7).

$$q = \frac{V_0}{nV_{IN}} = \frac{M}{n}$$
 (2.7)

Considering this, the duty cycle can be calculated for different turns ratio by the variation of the modulation index. Figure 19 presents the duty cycle calculated for n=1, 2, 3 and 4, respectively as $D_1(M)$, $D_2(M)$, $D_3(M)$ and $D_4(M)$, for the variation of the modulation index *M*.

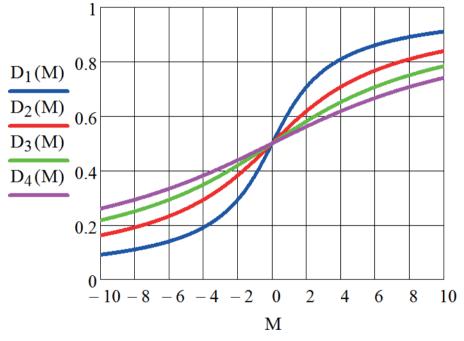


Figure 19 - Complementary switching strategy – modulation index vs duty cycle for different values of *n*. Source: Self-authorship

2.3 Magnetizing Inductances (L_{M1} and L_{M2})

To obtain the equations that determine the magnetizing inductances L_{M1} and L_{M2} , the relationship $V_L = {}^{L \cdot di}_{L}I_{dt}$ is used. For continuous conduction mode, the inductance values that guarantee a given specified current ripple (ΔI_{L1} and ΔI_{L2}) in the currents I_{LM1} and I_{LM2} are given by (2.8) and (2.9), respectively.

$$L_{M1} = \frac{V_{IN}D}{\Delta I_{L1}f_s}$$
(2.8)

$$L_{M2} = \frac{V_{IN} \left(1 - D\right)}{\Delta I_{L2} f_s}$$
(2.9)

Where *fs* is the switching frequency. From the converter analysis and considering that the output voltage frequency is much lower than the switching frequency, it is possible to compute the average values of I_{L1} and I_{L2} for every output current angle of α , as given by (2.10) and (2.11), respectively.

$$I_{L1}(\alpha) = \frac{I_o(\alpha)}{n(1 - D(\alpha))}$$
(2.10)

$$I_{L2}(\alpha) = \frac{I_o(\alpha)}{nD(\alpha)}$$
(2.11)

Both maximum and minimum levels of the current in the magnetizing inductance are derived from the values of I_{L_1} , I_{L_2} , ΔI_{L_1} and ΔI_{L_2} . Respectively, equations (2.12) and (2.13) provide the maximum and minimum values for the current in the magnetizing inductances.

$$I_{LK_{max}}(\alpha) = I_{LK}(\alpha) + \frac{\Delta I_{LK}}{2}$$
for $K = 1$ or 2
$$(2.12)$$

$$I_{LK_{min}}(\alpha) = I_{LK}(\alpha) - \frac{\Delta I_{LK}}{2}$$
for $K = 1$ or 2
$$(2.13)$$

From (2.8) it is possible to conclude that the maximum value of ΔI_{L1} occurs when *D* is maximum ($a = \pi/2$) and the maximum value of ΔI_{L2} occurs when *D* is minimum ($a = 3\pi/2$). In the particular case of a sinusoidal output voltage, it can be verified the validity of $D_{max} = (1 - D_{min})$. In this case, if $L_{M1} = L_{M2} = L_m$, the maximum values of ΔI_{L1} and ΔI_{L2} are equivalent, as given by (2.14).

$$\Delta I_{L1} = \Delta I_{L2} = \frac{V_{IN} D_{\text{max}}}{f_s L_m} = \frac{V_{IN} (1 - D_{\text{min}})}{f_s L_m}$$
(2.14)

2.4 Output Capacitors (C_A and C_B)

The value of the output capacitance is selected to ensure that the output voltage ripple is constrained within the required specification. The relationship $I_c = C \frac{dV}{dt}$ is used to

obtain the equation that determines the output capacitance of the converter. In steady state and continuous conduction mode, the output capacitances C_A and C_B are given by (2.15) and (2.16), respectively.

$$C_A = \frac{I_o D}{\Delta V_o f_s} \tag{2.15}$$

$$C_B = \frac{I_o(1-D)}{\Delta V_o f_s} \tag{2.16}$$

Where, I_o is the average value of the output current and ΔV_o is the output voltage ripple.

For a positive DC output voltage, the maximum voltage in capacitor C_A is given by (2.17).

$$V_{A} = V_{IN} n \frac{D}{(1-D)}$$
(2.17)

Whereas equation (2.18) gives the maximum voltage for C_{B} .

$$V_B = V_{IN} n \frac{(1-D)}{D} \tag{2.18}$$

For an alternate current operation, the maximum voltage across the output capacitor C_A occurs when $a = \pi/2$, in other words, the peak voltage over C_A occurs when the output voltage reaches its maximum value in the positive semi-cycle. Similarly, the maximum voltage across C_B occurs for $a = 3\pi/2$, when the output voltage reaches the minimum (most negative) value in the negative semi-cycle. Equations (2.19) and (2.20) give the average voltage over C_A and C_B , respectively, for any given angle value of the output voltage.

$$V_{A}(\alpha) = V_{IN} n \frac{D(\alpha)}{(1 - D(\alpha))}$$
(2.19)

$$V_{B}(\alpha) = V_{IN} n \frac{(1 - D(\alpha))}{D(\alpha)}$$
(2.20)

Therefore, the output voltage for both capacitors C_{A} and $C_{B'}$ with the converter operating an AC output, is given by (2.21).

$$V_{C0}(\alpha) = V_A(\alpha) - V_B(\alpha)$$
(2.21)

2.5 Switch S_{1P}

To specify the semiconductor technology used in the converter, maximum, RMS

and average current values, as well as the maximum voltage applied in each one of the semiconductors must be known.

Based on the theoretical waveforms presented in Figure 16, the average current in $S_{_{1P}}$ for a single switching period is determined by (2.22).

$$I_{S1P} = (I_{S1P\max} + I_{S1P\min})\frac{1}{2}D$$
(2.22)

The maximum current is obtained from the equation of the magnetizing inductance, defined by (2.8). Therefore, for $\Delta I_L = [I_{S1Pmax} - I_{S1Pmin}]$, I_{S1Pmax} is given by (2.23).

$$I_{S1P\max} = \frac{V_{IN}D}{L_M f_s} + I_{S1P\min}$$
(2.23)

Concerning the output current reflected to the primary, or $I_0.n$, and the relation that the average current in S_{1P} has with the input current I_{IN} , the equation that defines the current I_{S1Pmin} is given by (2.24).

$$I_{S1P\min} = \frac{I_o n}{(1-D)} - \frac{V_{IN}D}{2L_M f_s}$$
(2.24)

As the converter operates an AC output, the current I_{STPmin} assumes the variation of the output current as a product of the sinusoidal variation of the duty cycle, as presented in (2.25).

$$I_{S1P\min}(\alpha) = \frac{Io(\alpha)n}{(1-D(\alpha))} - \frac{V_{IN}D(\alpha)}{2f_s L_M}$$
(2.25)

The same applies to the current I_{S1Pmax} , as described by (2.26).

$$I_{S1P\max}(\alpha) = I_{S1P\min}(\alpha) + \frac{V_{IN}D(\alpha)}{f_sL}$$
(2.26)

To obtain the average current in $S_{_{1P}}$ from 0 to 2π , the equation that defines the line from $I_{_{S1Pmin}}$ to $I_{_{S1Pmax}}$ has to be known, as given by (2.27).

$$I_{S1P} = \frac{(I_{S1P\max} - I_{S1P\min})t}{DT_s} + I_{S1P\min}$$
(2.27)

If integrated from 0 to DT_s , as presented in (2.28), (2.27) results in (2.22).

$$I_{S1P} = \frac{1}{T_s} \int_0^{DT_s} \left(\frac{(I_{S1P\max} - I_{S1P\min})t}{DT_s} + I_{S1P\min} \right) dt$$
(2.28)

Thus, the average current in $S_{_{1P}}$ for an AC output is defined by the integral equation in (2.29).

$$I_{S1P_{AC}} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{(I_{S1P_{\text{max}}}(\alpha) + I_{S1P_{\text{min}}}(\alpha))D(\alpha)}{2} d\alpha$$
(2.29)

Regarding the RMS current in $S_{_{TP'}}$ in case of an alternate output operation, an equation is obtained from the RMS current definition applied to (2.28), which reads as given by (2.30).

$$I_{S1P_RMS} = \sqrt{\frac{1}{T_s} \int_0^{DT_s} \left(\frac{(I_{S1P\max} - I_{S1P\min})t}{DT_s} - I_{S1P\min} \right)^2 dt}$$
(2.30)

Resolve the integral presented in (2.30) to obtain (2.31).

$$I_{S1P_RMS} = \frac{1}{3}\sqrt{3}\sqrt{\left(I_{S1P\max}^2 + I_{S1P\max}I_{S1P\min} + I_{S1P\min}^2\right)D}$$
(2.31)

Finally, the RMS value of IS_{1P} can be obtained using the RMS definition from 0 to $_{2P}$ applied to (2.31), as given by (2.32).

$$I_{S1P_{RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{S1P\min}(\alpha)^{2} + I_{S1P\min}(\alpha)I_{S1P\max}(\alpha) + I_{S1P\max}(\alpha)^{2}\right)D(\alpha)}{3}} d\alpha \quad (2.32)$$

The maximum voltage across the switch also varies with the output voltage of the converter and it reaches a maximum value when $a = \frac{\eta}{2}$, as given by (2.33).

$$V_{S1P}(\alpha) = V_{IN} + \frac{V_A(\alpha)}{n} + \frac{\Delta V_0(\alpha)}{2}$$
(2.33)

Ultimately, the method adopted to obtain the equations that define the average and RMS current values presented in this section are used throughout this work for every component of the circuits presented.

2.6 Switch S_{1N}

Considering that $S_{_{1N}}$ is turned on during the second operating stage, the average current in $S_{_{1N}}$ according to the hatched area in Figure 16 for a voltage $V_o > 0$ is given by (2.34).

$$I_{S1N} = (I_{S1N\max} + I_{S1N\min})\frac{(1-D)}{2n}$$
(2.34)

The values of I_{S1Nmax} and I_{S1Nmin} are given by (2.35) and (2.36), respectively.

$$I_{S1N\max} = \frac{I_0 n}{D} + \frac{V_{IN} (1 - D)}{2L_M f_s}$$
(2.35)

$$I_{S1N\min} = \frac{I_o n}{D} - \frac{V_{IN} (1 - D)}{2L_M f_S}$$
(2.36)

For an AC output the current value of I_{S1Nmin} has its value dependent on the angle *a*, as presented in (2.37).

$$I_{S1N\min}\left(\alpha\right) = \frac{nI_{0}\left(\alpha\right)}{D\left(\alpha\right)} - \frac{V_{IN}\left(1 - D\left(\alpha\right)\right)}{2f_{s}L_{M}}$$
(2.37)

Therefore, in accordance to (2.35), I_{S1Nmax} (a) can be determined by (2.38).

$$I_{S1N\max}(\alpha) = \frac{I_0(\alpha)n}{D(\alpha)} + \frac{V_{IN}(1-D(\alpha))}{2f_s L_M}$$
(2.38)

The average value of the current in the switch $S_{_{1N}}$ in AC operation can be calculated by the integral in (2.39).

$$I_{S1N} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{(I_{S1N\max}(\alpha) + I_{S1N\min}(\alpha))(1 - D(\alpha))}{2} d\alpha$$
(2.39)

Equation (2.40) provides the RMS value of the current in S_{TN} .

$$I_{S1N_{RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{S1N_{max}}(\alpha)^{2} + I_{S1N_{max}}(\alpha)I_{S1N_{min}}(\alpha) + I_{S1N_{min}}(\alpha)^{2}\right) \left(1 - D(\alpha)\right)}{2} d\alpha}$$
(2.40)

The maximum voltage across S_{1N} is observed when the output voltage reaches its minimum in the negative semi-cycle ($V_0 < 0$) when $\alpha = {}^{3\pi} I_{2}$, as given by (2.41).

$$V_{S1N}(\alpha) = V_{IN} + \frac{V_B(\alpha)}{n} + \frac{\Delta V_0(\alpha)}{2}$$
(2.41)

2.7 Switch S_{2P}

Figure 20 shows that the current in the magnetizing inductance during the first operating stage circulates through $S_{_{1P}}$. During the second operating stage, the current $I_{_{LM1}}$ is reflected to the secondary winding, circulating through $S_{_{2P}}$ and transferring the energy to the output.

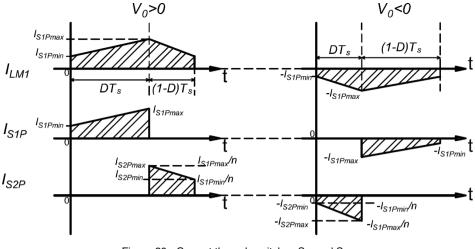


Figure 20 - Current through switches $S_{_{1P}}$ and $S_{_{2P}}$. Source: self-authorship

Therefore, a relation between the current in $S_{_{1P}}$ and $S_{_{2P}}$ in respect to the charge/ discharge of the magnetizing inductance can be described as given by (2.42) for $I_{_{S2Pmax}}$ and by (2.43) for $I_{_{S2Pmin}}$.

$$I_{S2P\max} = \frac{I_{S1P\max}}{n}$$
(2.42)

$$I_{S2P\min} = \frac{I_{S1P\min}}{n}$$
(2.43)

Similar to the previous switches, the average current value of $S_{_{2P}}$ is equal to the area under the trapezoidal form of the current in Figure 20. Thus, $I_{_{S2P}}$ can be determined by (2.44).

$$I_{S2P} = (I_{S2P\max} + I_{S2P\min})\frac{(1-D)}{2}$$
(2.44)

The values of I_{S2Pmin} and I_{S2Pmax} can be written in terms of alpha, as given by (2.45) and (2.46), respectively.

$$I_{S2P\min}(\alpha) = \frac{-I_{S1P\min}(\alpha)}{n}$$
(2.45)

$$I_{S2P\max}(\alpha) = \frac{-I_{S1P\max}(\alpha)}{n}$$
(2.46)

Therefore, equation (2.47) provides the means for calculating the average value of the current in $S_{_{2P}}$.

$$I_{S2P} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{(I_{S2P\max}(\alpha) + I_{S2P\min}(\alpha))(1 - D(\alpha))}{2} d\alpha$$
(2.47)

In a similar approach, one can determined the RMS value of I_{S2P} , as given by

$$I_{S2P_{RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{S2P\min}(\alpha)^{2} + I_{S2P\min}(\alpha)I_{S2P\max}(\alpha) + I_{S2P\max}(\alpha)^{2}\right)\left(1 - D(\alpha)\right)}{3}} d\alpha$$
(2.48)

The maximum voltage over switch S_{2P} is observed when $a = \frac{\eta}{2}$, in accordance to the result provided by (2.49).

$$V_{S2P}(\alpha) = V_{IN}n + V_A(\alpha) + \frac{\Delta V_0}{2}$$
(2.49)

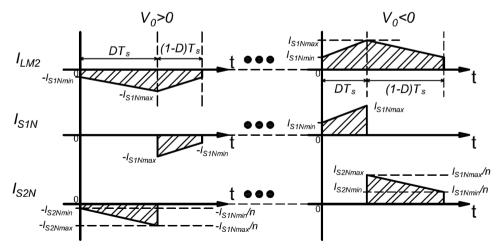
2.8 Switch S_{2N}

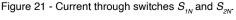
Figure 21 shows that the current in the magnetizing inductance during the second operating stage circulates through $S_{_{1N}}$. The current $I_{_{LM2}}$ is reflected to the secondary winding in the first operating stage, circulating through $S_{_{2N}}$ and transferring the energy to the output.

Therefore, a relation between the current in $S_{_{1N}}$ and $S_{_{2N}}$ in respect to the charge/ discharge of the magnetizing inductance can be described as given by (2.50) and (2.51), respectively, for $I_{_{S2Nmax}}$ and $I_{_{S2Nmin}}$.

$$I_{S2N\max} = \frac{I_{S1N\max}}{n}$$
(2.50)

$$I_{S2N\min} = \frac{I_{S1N\min}}{n}$$
(2.51)





Source: self-authorship

The average current value in $S_{_{2N}}$ based on the waveforms presented in Figure 21, is given by (2.52).

$$I_{S2N} = (I_{S2N_{max}} + I_{S2N_{min}})\frac{D}{2}$$
(2.52)

Equations (2.53) and (2.54), respectively, provide the minimum and maximum current values in $S_{_{2N}}$

$$I_{S2N\min}(\alpha) = \frac{I_{S1N\min}(\alpha)}{n}$$
(2.53)

$$I_{S2N\max}(\alpha) = \frac{I_{S1N\max}(\alpha)}{n}$$
(2.54)

The average current I_{S2N} for an AC output is given by (2.55).

$$I_{S2N} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{(I_{S2N\max}(\alpha) + I_{S2N\min}(\alpha))D(\alpha)}{2} d\alpha$$
(2.55)

The calculation of the RMS current values of I_{S2N} can be performed as presented in (2.56).

$$I_{S2N_{RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{S2N\min}(\alpha)^{2} + I_{S2N\min}(\alpha)I_{S2N\max}(\alpha) + I_{S2N\max}(\alpha)^{2}\right)D(\alpha)}{3}} d\alpha$$
(2.56)

The maximum voltage across switch S_{2N} is observed when a given by (2.57).

$$V_{S2N}(\alpha) = V_{IN}n + V_B(\alpha) + \frac{\Delta V_0}{2}$$
(2.57)

2.9 Small-signal Analysis for the Complementary Switching Strategy with Resistive Output Load

In this section, a transfer function is obtained for the converter operating with a resistive output load as depicted in Figure 22. In this work, the transfer functions obtained follow the small-signal analysis proposed by (ERICKSON, 1997).

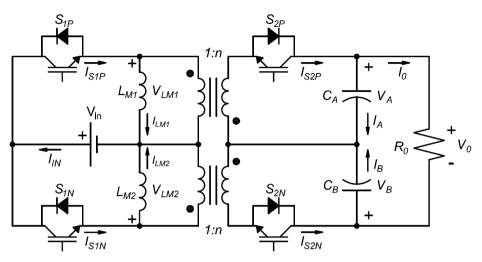


Figure 22 – DC-AC flyback converter with differential output connection operating a resistive load. Source: self-authorship

From the volt-second balance in the magnetizing inductances L_{M1} and L_{M2} , one can obtain equations (2.58) and (2.59).

$$\langle v_{LM1} \rangle = d(t) \langle V_{IN}(t) \rangle + d'(t) \langle \frac{-v_A}{n}(t) \rangle$$
 (2.58)

$$\langle v_{LM2} \rangle = d(t) \left\langle \frac{-v_B}{n}(t) \right\rangle + d'(t) \left\langle V_{IN}(t) \right\rangle$$
 (2.59)

Where d'(t) stands for (1 - d(t)).

Assuming that AC variations are much smaller than the respective quiescent values, the nonlinear equations (2.58) and (2.60) above can be linearized by perturbing the DC components (V_{INP} , V_A and V_B), resulting, respectively, in (2.61) and (2.62).

$$L_{M1}\left(\frac{dI_{LM1}}{dt} + \frac{di_{LM1}}{dt}\right) = \left[DV_{IN} - D'\frac{V_A}{n}\right] + \left[Dv_{IN} + dV_{IN} - D\frac{v_A}{n} + d\frac{v_A}{n}\right] + \left[\hat{d}v_{IN} + d\frac{v_A}{n}\right]$$

$$(2.61)$$

$$L_{M2}\left(\frac{dI_{LM2}}{dt} + \frac{d\dot{i}_{LM2}}{dt}\right) = \left[D'V_{IN} - D\frac{V_B}{n}\right] + \left[D'\dot{v}_{IN} - dV_{IN} - D\frac{\dot{v}_B}{n} - d\frac{V_B}{n}\right] + \left[\dot{d}\dot{v}_{IN} - d\frac{\dot{v}_B}{n}\right]$$
(2.62)

The small-signal equations are defined by the 1st order terms of the equations (2.61) and (2.62), determined as given by (2.63) and (2.64), respectively.

$$L_{M1}\frac{d\,i_{LM1}}{dt} = D\,\hat{v}_{IN} + \hat{d}\,V_{IN} - D\,\frac{v_A}{n} + \hat{d}\,\frac{V_A}{n}$$
(2.63)

$$L_{M2} \frac{d \, i_{LM2}}{dt} = D' \frac{v_{IN}}{n} - \hat{d} \frac{V_{IN}}{n} - D \frac{v_{B}}{n} - \hat{d} V_{IN}$$
(2.64)

The variable $\hat{v}_{_{IN}}$ is considered null from this point on because it is assumed that there will be no variation in the input voltage of the converter. Thus, the Laplace transform of equations (2.63) and (2.64), returns (2.65) and (2.66), respectively.

^

$$sL_{M1}i_{LM1}(s) = -D'\frac{v_A(s)}{n} + d(s)\frac{V_A}{n} + d(s)V_{IN}$$
(2.65)

$$sL_{M2}i_{LM2}(s) = -D\frac{v_B(s)}{n} - d(s)\frac{V_B}{n} - d(s)V_{IN}$$
(2.66)

Similarly, using the principles of the capacitor charge balance over one switching cycle, one obtain the equations (2.67) and (2.68).

$$\left\langle i_{CA}\right\rangle = d\left(t\right)\left\langle -i_{0}\left(t\right)\right\rangle + d'\left(t\right)\left\langle -i_{S2P}\left(t\right) - i_{0}\left(t\right)\right\rangle$$
(2.67)

$$\left\langle i_{CB} \right\rangle = d\left(t\right) \left\langle -i_{S2N}\left(t\right) + i_{0}\left(t\right) \right\rangle + d'\left(t\right) \left\langle i_{0}\left(t\right) \right\rangle$$
(2.68)

Applying perturbations to the equations (2.67) and (2.68), results in (2.69) and (2.70).

$$C_{A}\left(\frac{dV_{A}}{dt} + \frac{dv_{A}}{dt}\right) = \left[-D'I_{S2P} - I_{0}\right] + \left[-D'i_{S2P} + dI_{S2P} - i_{0}\right] + \left[di_{S2P}\right]$$
(2.69)

$$C_B\left(\frac{dV_B}{dt} + \frac{dv_B}{dt}\right) = \left[-D'I_{S2N} + I_o\right] + \left[-Di_{S2N} - dI_{S2N} + i_o\right] - \left[di_{S2N}\right]$$
(2.70)

The second order terms of (2.69) and (2.70) are neglected while the DC terms vanish as they satisfy the steady state analysis of the converter. The remaining 1st order terms in (2.69) and (2.70) are as shown, respectively, in (2.71) and (2.72).

$$C_{A}\frac{dv_{A}}{dt} = -D'\dot{i}_{S2P} + \dot{d}I_{S2P} - \dot{i}_{0}$$
(2.71)

$$C_{B} \frac{dv_{B}}{dt} = -D \dot{i_{S2N}} - d I_{S2N} + \dot{i_{0}}$$
(2.72)

Applying the Laplace transform in (2.71) and (2.72) result, respectively, in (2.73) and (2.74).

$$sC_{A}v_{A}(s) = -D'i_{S2P}(s) + d(s)I_{S2P} - i_{0}(s)$$
(2.73)

$$sC_{B}\hat{v}_{B}(s) = -D\hat{i}_{S2N}(s) - d\hat{s}I_{S2N} + \hat{i}_{0}(s)$$
(2.74)

The relation between $\hat{i}_{S2P}(s)$ and $\hat{i}_{LM1}(s)$ is described by (2.75) and the relation between $\hat{i}_{S2N}(s)$ and $\hat{i}_{LM2}(s)$ is presented in (2.76).

$$\hat{i}_{S2P}(s) = \frac{i_{LM1}(s)D'}{n}$$
 (2.75)

$$\dot{i}_{s_{2N}}(s) = \frac{\dot{i}_{LM2}(s)D}{n}$$
 (2.76)

Therefore, isolating the equations (2.65) and (2.73), in respect to the relation presented in (2.75), for \hat{i}_{LM} 1 (*s*), one obtains, respectively, (2.77) and (2.78).

$$\dot{i}_{LM1}(s) = -D'\frac{\dot{v}_{A}(s)}{sL_{M1}n} + \dot{d}(s)\frac{V_{A}}{sL_{M1}n} + \dot{d}(s)\frac{V_{IN}}{sL_{M1}}$$
(2.77)

$$\dot{i}_{LM1}(s) = \frac{sC_A v_A(s)n}{D'} + \frac{\dot{i}_0(s)n}{D'} + d(s)\frac{I_{LM1}}{D'}$$
(2.78)

And isolating both (2.66) and (2.74), in respect to (2.76) for $\hat{i}_{LM2}(s)$ give, respectively, (2.79) and (2.80).

Λ

$$\dot{i_{LM2}}(s) = -D\frac{v_B(s)}{sL_{M2}n} - \dot{d(s)}\frac{V_B}{sL_{M2}n} - \dot{d(s)}\frac{V_{IN}}{sL_{M2}}$$
(2.79)

$$\hat{i}_{LM2}(s) = \frac{sC_B v_B(s)n}{D} - \frac{\hat{i}_0(s)n}{D} - \hat{d}(s)\frac{I_{LM2}}{D}$$
(2.80)

By substituting (2.77) into (2.78) it is possible to derive (2.81),which provides the small-signal behavior of the voltage $\hat{v}_{_A}(s)$.

$$\hat{v}_{A}(s) = \hat{d}(s) \left[\frac{\left(V_{IN} + \frac{V_{A}}{n} \right) nD'}{D'^{2} + s^{2}L_{M1}C_{A}n^{2}} - \frac{sL_{M1}I_{LM1}n}{D'^{2} + s^{2}L_{M1}C_{A}n^{2}} \right] - \hat{i}_{0}(s) \left[\frac{sL_{M1}n^{2}}{D'^{2} + s^{2}L_{M1}C_{A}n^{2}} \right]$$
(2.81)

Similarly, substituting (2.79) into (2.80) gives the small-signal variation of the voltage across the output capacitor $C_{_{B'}}$ as given by (2.82).

$$-v_{B}(s) = \hat{d}(s) \left[\frac{\left(V_{IN} + \frac{V_{B}}{n} \right) nD}{D^{2} + s^{2} L_{M2} C_{B} n^{2}} - \frac{s L_{M2} I_{S2N} n}{D^{2} + s^{2} L_{M2} C_{B} n^{2}} \right] - \hat{i_{0}}(s) \left[\frac{s L_{M2} n^{2}}{D^{2} + s^{2} L_{M2} C_{B} n^{2}} \right]$$
(2.82)

Knowing that $L_{M1}=L_{M2}=L_M$ and $C_A=C_B=C_o$, one can determine (2.83) and (2.84)

$$\hat{v}_{A}(s) = \hat{d}(s) \left[\frac{\left(V_{IN} + V_{A} / n \right) n D'}{D'^{2} + s^{2} L_{M} C_{o} n^{2}} - \frac{s L_{M} I_{LM1} n}{D'^{2} + s^{2} L_{M} C_{o} n^{2}} \right] - \hat{i}_{0}(s) \left[\frac{s L_{M} n^{2}}{D'^{2} + s^{2} L_{M} C_{o} n^{2}} \right]$$
(2.83)

$$-v_{B}(s) = \hat{d}(s) \left[\frac{\left(V_{IN} + \frac{V_{B}}{n} \right) nD}{D^{2} + s^{2} L_{M} C_{o} n^{2}} - \frac{s L_{M} I_{S2N} n}{D^{2} + s^{2} L_{M} C_{o} n^{2}} \right] - \hat{i_{0}}(s) \left[\frac{s L_{M} n^{2}}{D^{2} + s^{2} L_{M} C_{o} n^{2}} \right]$$
(2.84)

From the converter analysis it is possible to verify the validity of (2.85).

$$v_0(s) = v_A(s) - v_B(s)$$
 (2.85)

Then, the small-signal variations of the output voltage can be considered $\hat{v}_0(s)$ by substituting (2.83) and (2.84) into (2.85)., which results in (2.86).

$$v_{0}(s) = \hat{d}(s) \left[\frac{\left(V_{IN} + V_{A}/n\right)nD}{D^{2} + s^{2}L_{M}C_{o}n^{2}} - \frac{sL_{M}I_{LM1}n}{D^{2} + s^{2}L_{M}C_{o}n^{2}} + \frac{\left(V_{IN} + V_{B}/n\right)nD}{D^{2} + s^{2}L_{M}C_{o}n^{2}} - \frac{sL_{M}I_{S2N}n}{D^{2} + s^{2}L_{M}C_{o}n^{2}} - \frac{sL_{M}I_{C}n^{2}}{D^{2} + s^{2}L_{M}C_{o}n^{2}} - \frac{sL_{M}I_{S2N}n}{D^{2} + s^{2}L_{M}C_{o}n^{2}} - \frac{sL$$

For the particular case of a resistive output load, where \hat{v}_0 (s) = \hat{l}_0 (s) R_o , the duty cycle to output current transfer function is given by (2.87).

$$G_{ds}(s) = \frac{i_0(s)}{d(s)} = \frac{B_3 s^3 + B_2 s^2 + B_1 s + B_0}{A_4 s^4 + A_3 s^3 + A_2 s^2 + A_1 s + A_0}$$
(2.87)

I

Where:

$$B_{3} = -L_{M}^{2}C_{o}n^{3}(I_{LM1} + I_{LM2})$$
$$B_{2} = L_{M}C_{o}n^{3}[V_{A} - V_{A}D + V_{IN}n + V_{B}D]$$

۸

$$B_{1} = -L_{M} n \left(D^{2} I_{LM1} + I_{LM2} - 2DI_{LM2} + D^{2} I_{LM2} \right)$$

$$B_{0} = (1 - D) D \left[V_{A} D + V_{B} - V_{B} D + V_{IN} n \right]$$

$$A_{4} = L_{M}^{2} C_{o}^{2} n^{4} R_{o}$$

$$A_{3} = 2L_{M}^{2} C_{o} n^{4}$$

$$A_{2} = L_{M} C_{o} n^{2} R_{o} \left(D^{2} + (1 - D)^{2} \right)$$

$$A_{1} = L_{M} n^{2} \left(D^{2} + (1 - D)^{2} \right)$$

$$A_{0} = R_{o} (1 - D)^{2} D^{2}$$

2.10 Small-signal Analysis for the Complementary Switching Strategy Coupled to an Output Voltage Source

It is possible to divide the spectrum of the converter in two portions, one related to the fundamental frequency harmonics and the other that concerns the switching harmonics (CALZO, LIDOZZI, *et al.*, 2013). The alternate output voltage/current operates in the fundamental frequency of the grid, but the ripple of this output presents undesired frequencies that are related to the converter switching behavior. The analysis presented in section 2.2.9 for an output linear load is not well suited for grid- tied applications because of the intrinsic high-frequency harmonics caused by the switching frequency of the semiconductors. Therefore, a filter is needed for reducing the high-frequency harmonics, allowing low frequencies to pass through, at the output of the converter. Figure 23 presents the circuit of the converter with an inductive filter to reduce the high-frequency harmonics.

The operating stages of the converter remains the same, although the voltage across the output inductive filter must be analyzed.

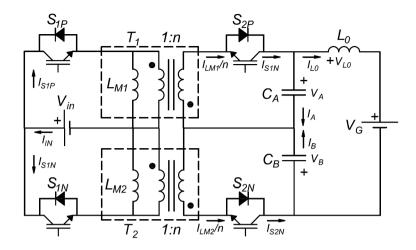


Figure 23 – Complementary switching strategy coupled to an output voltage source. Source: Self-authorship

In the first operating stage (Figure 24), what differs from the analysis presented in section 0 is that the current previously identified as I_o is identified here as I_{L0} to indicate the presence of the inductive filter. Therefore, the voltage on L_o is obtained from the mesh analysis of the circulating current I_{L0} , which gives (2.88).

$$V_{L0} = V_A - V_B - V_G \tag{2.88}$$

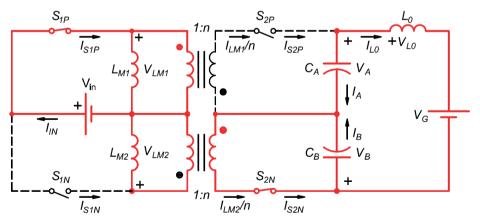


Figure 24 - 1st operating stage - complementary switching strategy coupled to an output voltage source. Source: Self-authorship

The same considerations of magnetizing inductances' voltages and capacitors' currents are valid for the second operating stage (Figure 25). The resultant voltage $V_{\mu a}$ from

the mesh analysis of I_{μ} is the same as the voltage presented in (2.88).

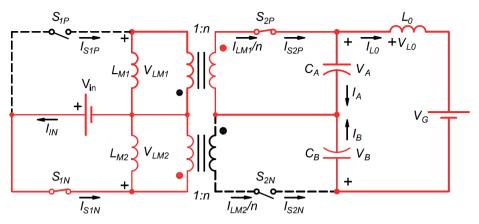


Figure $25 - {}_{2N}{}^{d}$ operating stage - complementary switching strategy coupled to an output voltage source. Source: Self-authorship

Under these conditions, the volt-second balance on the magnetizing inductances L_{M1} and L_{M2} remain the same as respectively presented in equations (2.58) and (2.59). Thus, the frequency domain equations with the 1st order small-signal components are also the same as (2.65) and (2.66).

The capacitor charge balance of C_A and C_B return the same equations as well, although the name of the current I_o presented in (2.67) and (2.68), changed to I_{Lo} , as presented in (2.89) and (2.90), respectively.

$$\langle i_{CA} \rangle = d(t) \langle -i_{L0}(t) \rangle + d'(t) \langle \frac{-i_{LM1}(t)}{n} - i_{L0}(t) \rangle$$
 (2.89)

$$\langle i_{CB} \rangle = d(t) \left\langle \frac{-i_{LM2}(t)}{n} + i_{L0}(t) \right\rangle + d'(t) \langle i_{L0}(t) \rangle$$
 (2.90)

The linearization of (2.89) and (2.90) results in (2.91) and (2.92), respectively.

$$C_{A}\left(\frac{dV_{A}}{dt} + \frac{d\dot{v}_{A}}{dt}\right) = \left[-D'\frac{I_{LM1}}{n} - I_{L0}\right] + \left[-D'\frac{\dot{i}_{LM1}}{n} + \dot{d}\frac{I_{LM1}}{n} - \dot{i}_{L0}\right] + \left[\dot{d}\frac{\dot{i}_{LM1}}{n}\right]$$
(2.91)

$$C_B\left(\frac{dV_B}{dt} + \frac{d\dot{v_B}}{dt}\right) = \left[-D'\frac{I_{LM2}}{n} + I_{L0}\right] + \left[-D\frac{\dot{i_{LM2}}}{n} - \dot{d}\frac{I_{LM2}}{n} + \dot{i_{L0}}\right] - \left[\dot{d}\frac{\dot{i_{LM2}}}{n}\right]$$
(2.92)

Neglecting the second order terms and knowing that the DC terms of (2.91) and

(2.92) will vanish, it is possible to determine equations (2.93) and (2.94), respectively.

$$sC_{A}v_{A}(s) = -D'i_{LM1}(s) + \hat{d}(s)\frac{I_{LM1}}{n} - i_{L0}(s)$$
(2.93)

$$sC_{B}\dot{v}_{B}(s) = -D\frac{\dot{i}_{LM2}(s)}{n} - d(s)\frac{I_{LM2}}{n} + \dot{i}_{L0}(s)$$
(2.94)

Finally, the Volt-second balance of the output inductive filter is defined by (2.95).

$$\left\langle v_{L0}\right\rangle = \left\langle v_A - v_B - V_G\right\rangle \tag{2.95}$$

Perturb (2.95) to notice that only the voltage constants and first order terms remain in the equation, as given by (2.96).

$$L_{0} \frac{d i_{LG}}{dt} = \left[V_{A} - V_{B} - V_{0} \right] + \left[\dot{v}_{A} - \dot{v}_{B} + \dot{v}_{G} \right]$$
(2.96)

Considering that no small-signal variations are expected at the grid voltage (*VG*), the variable $\hat{v}_{_G}$ is neglected from this point onwards. Therefore, the equation on the frequency domain obtained from the Laplace transform of the first order terms of equation (2.96) and presented in (2.97).

$$sL_0 \dot{i}_{L0}(s) = \dot{v}_A(s) - \dot{v}_B(s)$$
 (2.97)

The equations presented, result in a system of five equations and five unknown variables, namely $\hat{v}_{A}(s)$, $\hat{v}_{B}(s)$, $\hat{i}_{LM1}(s)$, $\hat{i}_{LM2}(s)$ and $\hat{i}_{L0}(s)$, as presented in (2.98).

$$\begin{cases} sL_{M1}i_{LM1}(s) = -D'\frac{v_{A}(s)}{n} + d(s)\frac{V_{A}}{n} + d(s)V_{IN} \\ sL_{M2}i_{LM2}(s) = -D\frac{v_{B}(s)}{n} - d(s)\frac{V_{B}}{n} - d(s)V_{IN} \\ sC_{A}v_{A}(s) = -D'i_{LM1}(s) + d(s)\frac{I_{LM1}}{n} - i_{L0}(s) \\ sC_{B}v_{B}(s) = -D\frac{i_{LM2}(s)}{n} - d(s)\frac{I_{LM2}}{n} + i_{L0}(s) \\ sL_{0}i_{L0}(s) = v_{A}(s) + v_{B}(s) \end{cases}$$
(2.98)

The desired control to output transfer function is obtained by eliminating the unknown variables of the system of equations presented in (2.98) in order to obtain the transfer function presented in (2.99).

$$\frac{i_{L0}(s)}{\hat{d}(s)} = \frac{B_3 s^3 + B_2 s^2 + B_1 s + B_0}{A_5 s^5 + A_4 s^4 + A_3 s^3 + A_2 s^2 + A_1 s + A_0}$$
(2.99)

Where:

$$B_{3} = -C_{o}L_{M}^{2}n^{3}(I_{LM1} + I_{LM2})$$

$$B_{2} = C_{o}L_{M}n^{2}(V_{IN}n + DV_{B} + (1-D)V_{A})$$

$$B_{1} = -L_{M}n(I_{LM1}D^{2} + I_{LM2}(1-D)^{2})$$

$$B_{0} = D(1-D)(V_{IN}n + (1-D)V_{B} + DV_{A})$$

$$A_{5} = C_{o}^{2}L_{M}^{2}L_{0}n^{4}$$

$$A_{4} = 0$$

$$A_{3} = 2C_{o}L_{M}^{2}n^{4} + C_{o}L_{M}L_{0}D^{2}n^{2} + C_{o}L_{M}L_{0}(1-D)^{2}n^{2}$$

$$A_{2} = 0$$

$$A_{1} = L_{M}D^{2}n^{2} + L_{M}(1-D)^{2}n^{2} + L_{0}D^{2}(1-D)^{2}$$

3 | ALTERNATIVE SWITCHING STRATEGY

For a positive voltage output (*V0>0*), the alternative switching method consists in switching $S_{_{1P}}$ in DT_s seconds and $S_{_{2P}}$ in (1-D)Ts seconds, while keeping switch $S_{_{2N}}$ on for the whole positive semi-cycle and $S_{_{1N}}$ off. For a negative voltage output ($V_o<0$), switch $S_{_{1N}}$ is triggered in DT_s and $S_{_{2N}}$ in (1-D) T_s , witch switch $S_{_{1P}}$ on for the whole negative semi-cycle and $S_{_{1P}}$ off. Figure 26 shows the switching signal for the alternative switching strategy and the respective voltage at the output of the converter.

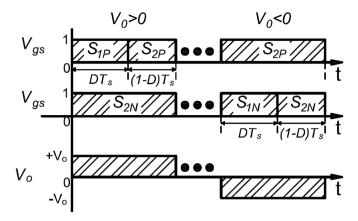


Figure 26- Switching signals and output voltage for the alternative switching strategy. Source: self-authorship

The main advantage of this switching strategy lies on the alternative path that the output current finds through the secondary winding of the flyback inductor when either $S_{_{2N}}$ is on, during the positive semi-cycle, or $S_{_{2P}}$ is on, during the negative semi-cycle. In other words, this switching strategy spares the converter from the switching losses descendant from the complementary switching strategy between $S_{_{1N}}$ and $S_{_{2N}}$ when $V_o > 0$ and between $S_{_{1P}}$ and $S_{_{2P}}$ when $V_o < 0$. By implementing this switching strategy, due to the reduction of switching losses and RMS current values in all four switches, higher efficiency levels are expected. However, due its complexity, the implementation of this switching strategy requires better hardware, whilst the complementary switching strategy can be performed with simple solutions.

3.1 Operating Stages for the Alternative Switching Strategy

The DC-AC flyback converter with differential output connection operating with the alternative switching strategy in continuous conduction mode (CCM) has a total of four different operating stages, although only two by semi-cycle of the output voltage. It means that there are a first and a second operating stages for a positive semi-cycle (V_{o} >0) and another first and second operating stages for a negative semi-cycle (V_{o} <0).

During the first operating stage for $V_{o}>0$, switch S_{1P} is turned on, charging the magnetizing inductance L_{M1} . Capacitor C_{A} discharges to the output load through switch S_{2N} and the secondary winding of the flyback inductor. Figure 27 highlights the equivalent circuit during the first operating stage for $V_{o}>0$.

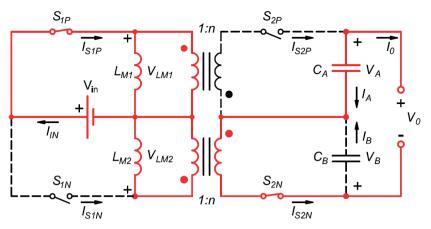


Figure 27 – 1st operating stage for the alternative switching strategy ($V_o > 0$). Source: self-authorship

In the second operating stage for $V_o > 0$, S_{1P} turns off, S_{2P} turns on and S_{2N} remains on. During this stage, the energy stored in the magnetizing inductance L_{M1} is transferred to the secondary of the flyback inductor and to the output through S_{2P} . With both S_{2P} and S_{2N} turned on, the output voltage V_o is reflected to the primary winding of the flyback inductor over the magnetizing inductance L_{M1} . The equivalent circuit of the second operating stage for $V_o > 0$ is presented in Figure 28.

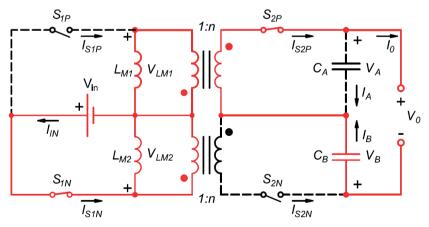


Figure 28 – 2^{Nd} operating stage for the alternative switching strategy ($V_{o}>0$). Source: self-authorship

When the voltage output crosses zero and becomes negative ($V_o < 0$), the operating stages of the converter are symmetrical but different from the ones presented in Figure 27 and Figure 28. In the first operating stage for $V_o < 0$, S_{1N} is turned on, charging the magnetizing inductance L_{M2} . The output capacitor C_B discharges to the output load through switch S_{2P} .

which is on, and the secondary winding of the flyback inductor. Figure 29 highlights the equivalent circuit for the first operating stage when $V_a < 0$.

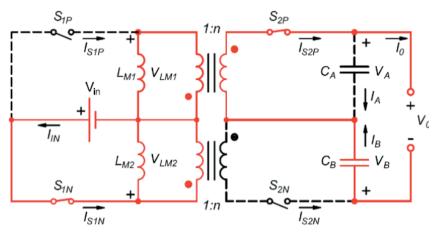


Figure 29 – 1st operating stage for the alternative switching strategy ($V_0 < 0$). Source: self-authorship

During the second operating stage for $V_0 < 0$, switch S_{1N} turns off, S_{2N} turns on and S_{2P} remains on. The energy stored in the magnetizing inductance L_{M2} is transferred to the secondary winding of the flyback inductor and to the output. Considering that both switches S_{2P} and S_{2N} are on, the output voltage V_0 is reflected to the magnetizing inductance L_{M2} . The equivalent circuit of this operating stage is shown in Figure 30.

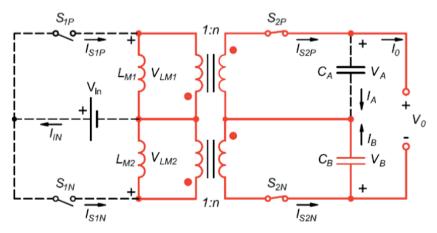


Figure $30 - 2^{Nd}$ operating stage for the alternative switching strategy ($V_0 < 0$). Source: self-authorship

It is noteworthy that the implementation of this switching strategy is only possible if there is a dead time between the operating stages of the converter, so there is no overlap of the control pulses to the switches, which causes short circuit between the primary and secondary windings of the flyback inductor. However, neither the dead time nor the impact it possibly has on the converter are considered for the analysis of the operating stages.

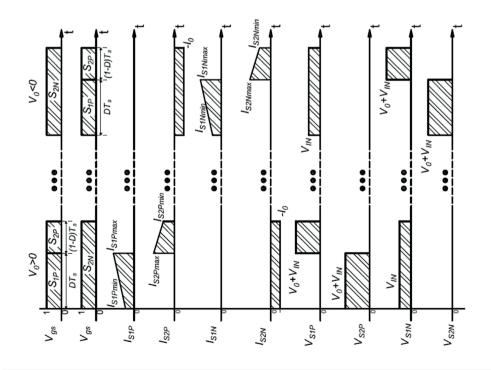
From the analysis of the two operating stages for $V_o > 0$, the voltages across the magnetizing inductances L_{M1} and L_{M2} and the currents through the output capacitors C_A and C_B are determined as shown in Table 2.

1 st Power Stage	2 nd Power Stage
$V_{L1} = V_{IN}$	$V_{L1} = \frac{-V_o}{n}$
$V_{L2} = 0$	$V_{L2} = 0$
$I_{CA} = -I_o$	$I_{CA} = I_{S2P} - I_o$
$I_{CB} = 0$	$I_{CB} = 0$

Table 2 – Magnetizing inductances' voltages and output capacitors' current – alternative switching strategy.



The theoretical waveforms derived from the analysis of the operating stages are presented in Figure 31.



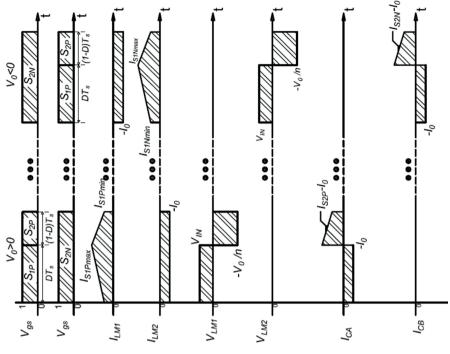


Figure 31 – Theoretical waveforms of the alternative switching strategy Source: self-authorship

3.2 Static Analysis – Alternative Switching Strategy

Assuming that the voltage conversion ratio q derives from the voltage levels over the magnetizing inductances (L_{M1} and L_{M2}) during both operating stages for either $V_0 > 0$ or $V_0 < 0$, q(t) is defined by (2.100).

$$q = \frac{V_0}{V_{IN}} = \frac{nD}{(1-D)}$$
(2.100)

Isolating D in (2.100) results in the equation of the duty cycle that ensures the operation with a given voltage conversion ratio, as presented in (2.101).

$$D = \frac{V_0}{nV_{IN} + V_0} = \frac{q}{(1+q)}$$
(2.101)

Similar to the previous modulation analysis, a sinusoidal behavior is expected at the output of the converter. Replacing (2.5) into (2.101) gives (2.102), which determines the duty cycle value that ensures a sinusoidal output voltage for any given angle alpha.

$$D(\alpha) = \frac{V_p \sin(\alpha)}{nV_{IN} + V_p \sin(\alpha)}$$
(2.102)

Considering that from π to 2π the duty cycle of $S_{_{1P}}$ has to be zero and $S_{_{2P}}$ has to be one, the equation that defines the duty cycle for these switches have to obey the conditions set by (2.103).

$$D_{P}(\alpha) = \begin{cases} \frac{q(\alpha)}{1+q(\alpha)} \to \alpha < \pi \\ 0 \to \pi < \alpha < 2\pi \end{cases}$$
(2.103)

Similarly, switches $S_{_{1N}}$ and $S_{_{2N}}$ have to obey the opposite conditions that defines the duty cycle for $S_{_{1P}}$ and $S_{_{2P}}$ to guarantee the symmetry of the converter, as given by (2.104).

$$D_{N}(\alpha) = \begin{cases} \frac{-q(\alpha)}{1-q(\alpha)} \to \pi < \alpha < 2\pi \\ 0 \to \alpha < \pi \end{cases}$$
(2.104)

Therefore, peak positive output voltage is obtained for $a = \frac{n}{2}$ from equation

$$V_{pk_{-}POS}(\alpha) = \frac{D_{p}(\alpha)V_{IN}n}{(1-D(\alpha))}$$
(2.105)

Similarly, peak negative output voltage is obtained by evaluating (2.106) at $a = \frac{3\pi}{2}$.

$$V_{pk_NEG}(\alpha) = -\frac{D_N(\alpha)V_{IN}n}{(1-D_N(\alpha))}$$
(2.106)

Figure 32 presents the resulting curve of the duty cycle as the voltage conversion ratio increases, given by equations (2.103) and (2.104).

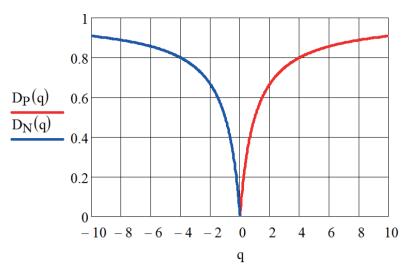


Figure 32 - Alternative switching strategy - voltage conversion ratio vs duty cycle. Source: Self-Authorship

As the duty cycle depends on the modulation index *M*, given by (2.107), different duty cycles can be found for different values of *n*. Figure 33 presents the variation of the duty cycle $D_{P1}(M)$, $D_{P2}(M)$ and $D_{P3}(M)$, respectively for *n=1, 2* and *3*, considering a positive output voltage.

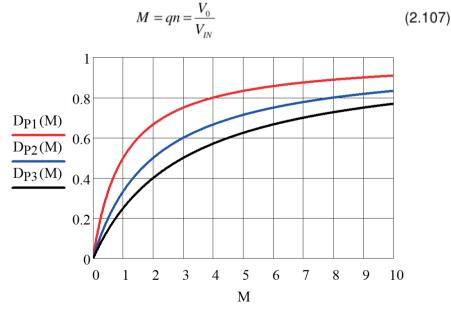
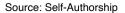


Figure 33 - Alternative switching strategy – positive modulation index vs duty cycle for different values of *n*.



3.3 Magnetizing Inductances (L_{M1} and L_{M2})

In continuous conduction mode, during the first operating stage, the voltage across the inductor $L_{_{M1}}$ is given by (2.108).

$$V_{LX}(t) = L_X \frac{dI_L}{dt} = V_{IN}$$
(2.108)

In order to guarantee a maximum current ripple, L_{M1} is calculated according to (2.109). Due to the converter symmetry, L_{M2} must have the same inductance value as L_{M1} .

$$L_{M1} = L_{M2} = \frac{V_{IN} D_P \left(\frac{\pi}{2}\right)}{\Delta I_{LM} f_s}$$
(2.109)

Using the principles of the capacitor charge balance in C_{A} , one can determine

$$I_{CA} = D_{P} (-I_{0}) + (1 - D_{P}) (nI_{LM1} - I_{0})$$

$$0 = -D_{P}I_{0} + (1 - D_{P}) (nI_{LM1} - I_{0})$$

$$0 = nI_{LM1} - I_{0} - D_{P}nI_{LM1}$$

(2.110)

Solving (2.110) results in (2.111), which can be used to determine the average current through $L_{_{M1}}$ within a switching cycle for a given angle alpha. A similar analysis can be carried out for $C_{_{R2}}$ resulting in the average value of $IL_{_{M2}}$ as given in (2.112).

$$I_{LM1}(\alpha) = \frac{I_0(\alpha)}{n(1 - D_P(\alpha))}$$
(2.111)

$$I_{LM2}(\alpha) = \frac{I_0(\alpha)}{n(1 - D_N(\alpha))}$$
(2.112)

The maximum and minimum values of the current in the magnetizing inductance can be derived from the values of I_L and ΔI_L . Equations (2.12) and (2.13), respectively, presents the maximum and minimum magnetizing current values.

From (2.109) it is possible to conclude that the maximum value of ΔI_{LM1} occurs when D_p is maximum ($\alpha = \pi/2$) and the maximum value of ΔI_{L2} occurs when D_N is maximum ($\alpha = 3\pi/2$).

3.4 Output Capacitors (C_A and C_B)

During the first switching stage, the current in the output capacitor C_A is determined by (2.113).

$$I_{CA} = C_A \frac{dV_{CA}}{dt} = -I_0$$
 (2.113)

Integrating (2.113) over the duration of the first stage yields (2.114).

$$C_A = \frac{I_0 D_P}{\Delta V_0 f_s} \tag{2.114}$$

When the converter operates with alternate output voltage, C_A and C_B are equal and determined by the equations (2.115) and (2.116).

$$C_{A} = \frac{I_{0}\left(\frac{\pi}{2}\right)D_{P}\left(\frac{\pi}{2}\right)}{\Delta V_{0}f_{s}}$$
(2.115)

$$C_{B} = \frac{I_{0}\left(\frac{3\pi}{2}\right)D_{N}\left(\frac{3\pi}{2}\right)}{\Delta V_{0}f_{s}}$$
(2.116)

3.5 Switch S_{1P}

Based on the theoretical waveform of the current in $S_{_{1P}}$ (see Figure 31), the current $I_{_{S1Pmin}}$ for a given angle alpha, imposed by the variation of the duty cycle $D_{_{P}}(a)$, can be determined by (2.117).

$$I_{S1P\min}\left(\alpha\right) = \frac{nI_{o}\left(\alpha\right)}{\left(1 - D_{P}\left(\alpha\right)\right)} - \frac{V_{IN}D_{P}\left(\alpha\right)}{2f_{s}L_{M}}$$
(2.117)

Similarly, $IS_{1P}max$ has its value in accordance with (2.118).

$$I_{S1P\max}(\alpha) = I_{S1P\min}(\alpha) + \frac{V_{IN}D_P(\alpha)}{f_s L_M}$$
(2.118)

The average value of the current through $S_{_{1P}}$ can be calculated over a period of the output voltage by the integral equation (2.119).

$$I_{S1P}(\alpha) = \frac{1}{2\pi} \int_{0}^{\pi} \frac{\left(I_{S1P\max}(\alpha) + I_{S1P\min}(\alpha)\right) D_{P}(\alpha)}{2} d\alpha$$
(2.119)

Notice that the integral is evaluated is from zero to p because $S_{_{1P}}$ is turned off from p to 2π . Therefore, the RMS current $I_{_{S1P} RMS}$ is given by (2.120).

$$I_{S1P_{RMS}}(\alpha) = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{S1P\min}(\alpha)^{2} + I_{S1P\min}(\alpha)I_{S1P\max}(\alpha) + I_{S1P\max}(\alpha)^{2}\right)D_{p}(\alpha)}{3}} d\alpha}$$
(2.120)

The voltage across S_{TP} for any given value of α is determined by (2.121).

$$V_{S1P}(\alpha) = V_{IN} + \frac{V_{pk_POS}(\alpha)}{n}$$
(2.121)

Both current and voltage reach its maximum values in S_{1P} when $a = \frac{n}{2}$.

3.6 Switch S₂

The value of the current I_{S2Pmin} with a given value of α is calculated as shown in (2.122).

$$I_{S2P\min}(\alpha) = \frac{I_o(\alpha)}{(1 - D_P(\alpha))} - \frac{V_{IN}D_P(\alpha)}{2f_s L_M}$$
(2.122)

Equation (2.123) provides the maximum current for S_{2P} .

$$I_{S2P\max}(\alpha) = I_{S2P\min}(\alpha) + \frac{V_{IN}D_P(\alpha)}{f_s L_M}$$
(2.123)

On solving the integral equation (2.124), one can determine the average value of the current through $S_{_{2P}}$. It is noteworthy that this value takes into consideration an alternate output voltage waveform.

$$I_{S2P}(\alpha) = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{(I_{S2P_{-}\max}(\alpha) + I_{S2P_{-}\min}(\alpha))(1 - D_{P}(\alpha))}{2} d\alpha$$
(2.124)

Regarding the RMS value of I_{S2P} , it can be derived from equation (2.125).

$$I_{S2P_{-RMS}}(\alpha) = \sqrt{\frac{n^2}{2\pi}} \int_{0}^{2\pi} \frac{(I_{S2P\max}(\alpha)^2 + I_{S2P\max}(\alpha)I_{S2P\min}(\alpha) + I_{S2P\min}(\alpha)^2)(1 - D_P(\alpha))}{3} d\alpha$$

Considering a particular value of alpha, the voltage across S_{2P} has its value given by (2.126).

$$V_{S2P}(\alpha) = V_{IN}n + V_{pk_{POS}}(\alpha)$$
(2.126)

3.7 Switch *S*_{1N}

Taking into consideration that the two operating stages for $V_0 > 0$ produces the same equations as the two operating stages for $V_0 < 0$, confirmed by the voltage conversion ratio q(t), the equations of the currents and voltages for S_{1N} are similar to the equations defined for S_{1P} . The difference lies in the duty cycle equation, the former defined for D_N in (2.104) and the latter defined for D_P in (2.103). Thus, the maximum values for currents and voltages in S_{1N} are observed when D_N is maximum, which occurs at $3\pi/2$.

Therefore, resembling the equation presented in (2.117), the current I_{S1Nmin} is given

(2.125)

by (2.127).

$$I_{S1N\min}(\alpha) = \frac{nI_0(\alpha)}{(1 - D_N(\alpha))} - \frac{V_{IN}D_N(\alpha)}{2f_sL_M}$$
(2.127)

In a similar manner, one can determine I_{S1Nmax} as given by (2.128).

$$I_{S1N\max}(\alpha) = I_{S1N\min}(\alpha) + \frac{V_{IN}D_N(\alpha)}{f_sL_M}$$
(2.128)

The average value of the current through $S_{_{1N}}$ is determined by solving (2.129)

$$I_{S1N}(\alpha) = \frac{1}{2\pi} \int_{0}^{\pi} \frac{\left(I_{S1N\max}(\alpha) + I_{S1N\min}(\alpha)\right) D_{N}(\alpha)}{2} d\alpha$$
(2.129)

Equation (2.130) provides the means for calculating the RMS value of S_{1N}

$$I_{S1N_{-}RMS}(\alpha) = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{S1N\min}(\alpha)^{2} + I_{S1N\min}(\alpha)I_{S1N\max}(\alpha) + I_{S1N\max}(\alpha)^{2}\right)D_{N}(\alpha)}{3}} d\alpha$$
(2.130)

Finally, the voltage across S_{1N} for a given alpha obeys (2.131).

$$V_{S1N}(\alpha) = V_{IN} + \frac{V_{pk_NEG}(\alpha)}{n}$$
(2.131)

3.8 Switch S_{2N}

 $S_{_{2N}}$

The considerations made for $S_{_{1N}}$ regarding the duty cycle and the similarity between $S_{_{1N}}$ and $S_{_{2P}}$ are valid for $S_{_{2N}}$ and $S_{_{2P}}$ as well. Thus, the current $I_{_{S2Nmin}}$ is given by (2.132).

$$I_{S2N\min}(\alpha) = \frac{I_o(\alpha)}{(1 - D_N(\alpha))} - \frac{V_{IN}D_N(\alpha)}{2f_sL_M}$$
(2.132)

The maximum current value I_{S2Nmax} , used to define the average and RMS current values in $S_{2N'}$ can be determined by (2.133).

$$I_{S2N\max}(\alpha) = I_{S2N\min}(\alpha) + \frac{V_{IN}D_N(\alpha)}{f_sL_M}$$
(2.133)

The average current value of I_{S2N} results from the solution of (2.134).

$$I_{S2N}(\alpha) = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{(I_{S2N\max}(\alpha) + I_{S2N\min}(\alpha))(1 - D_N(\alpha))}{2} d\alpha$$
(2.134)

The integral equation (2.135) is used to derive the RMS value of the current through

$$I_{S2N_{RMS}}(\alpha) = \sqrt{\frac{n^{2}}{2\pi} \int_{0}^{2\pi} \left(\frac{I_{S2N_{max}}(\alpha)^{2} + I_{S2N_{max}}(\alpha)I_{S2N_{min}}(\alpha) + I_{S2N_{min}}(\alpha)^{2} \right) (1 - D_{N}(\alpha))}{3} d\alpha}$$

The voltage on S_{2N} for any given α is given by (2.136).

$$V_{S2N}(\alpha) = V_{IN}n + V_{pk_NEG}(\alpha)$$
(2.136)

(2.135)

3.9 Small-signal Analysis for the Alternative Switching Strategy with Resistive Output Load

From the Volt-second balance in the magnetizing inductances $L_{_{M1}}$ and $L_{_{M2}}$, one can obtain the equations (2.137) and (2.138).

$$\langle v_{LM1}(t) \rangle = d(t) \langle v_{IN}(t) \rangle + d'(t) \langle \frac{-v_A(t)}{n} \rangle$$
 (2.137)

$$\left\langle v_{LM2}(t)\right\rangle = d(t)\left\langle v_{IN}(t)\right\rangle + d'(t)\left\langle \frac{-v_B(t)}{n}\right\rangle$$
 (2.138)

Applying small perturbations on (2.137) and (2.138) yields, respectively, (2.139) and (2.140).

$$L_{M1}\left(\frac{di_{LM1}}{dt} + \frac{di_{LM1}}{dt}\right) = \left[DV_{IN} - D'\frac{V_A}{n}\right] + \left[Dv_{IN} + dV_{IN} - D'\frac{v_A}{n} + d\frac{V_A}{n}\right] + \left[\hat{d}v_{IN} + d\frac{v_A}{n}\right]$$
(2.139)

$$L_{M2}\left(\frac{dI_{LM2}}{dt} + \frac{di_{LM2}}{dt}\right) = \left[-\frac{V_B}{n}\right] + \left[-\frac{v_B}{n}\right]$$
(2.140)

Ignoring second-order terms and knowing that the DC terms will vanish, on can determine the linearized small-signal equations (2.141) and (2.142).

$$L_{M1}\frac{d\,i_{LM1}}{dt} = D\,\hat{v_{IN}} + \hat{d}\,V_{IN} - D'\frac{\hat{v_A}}{n} + \hat{d}\frac{V_A}{n}$$
(2.141)

$$L_{M2}\frac{d\,\hat{i}_{LM2}}{dt} = -\frac{\hat{v}_{B}}{n} \tag{2.142}$$

Applying the Laplace transform to (2.141) and (2.142) and neglecting perturbations on $\hat{v}_{_{IN}}$, results in (2.143) and (2.144), respectively.

$$sL_{M1}\dot{i}_{LM1}(s) = \dot{d}(s)V_{IN} - D'\frac{v_A(s)}{n} + \dot{d}(s)\frac{V_A}{n}$$
(2.143)

$$sL_{M2}\dot{i}_{LM2}(s) = -\frac{v_B(s)}{n}$$
 (2.144)

From the principles of capacitor charge balance, the equations (2.145) and (2.146) are obtained for $C_{\!_A}$ and $C_{\!_B}$.

$$\left\langle i_{CA}\left(t\right)\right\rangle = d\left(t\right)\left\langle -i_{0}\left(t\right)\right\rangle + d'\left(t\right)\left\langle \frac{i_{LM1}\left(t\right)}{n} - i_{0}\left(t\right)\right\rangle$$
(2.145)

$$\left\langle i_{CB}(t)\right\rangle = d\left(t\right) \left\langle \frac{i_{LM2}\left(t\right)}{n} + i_{0}\left(t\right) \right\rangle + d'\left(t\right) \left\langle \frac{i_{LM2}\left(t\right)}{n} + i_{0}\left(t\right) \right\rangle$$
(2.146)

Equations (2.147) and (2.148) are determined by applying small perturbations to (2.145) and (2.146), respectively.

$$C_{A}\left(\frac{dV_{A}}{dt} + \frac{d\dot{v}_{A}}{dt}\right) = \left[D'I_{S2P} - I_{0}\right] + \left[D'\frac{\dot{i}_{LM1}}{n} - \dot{i}_{0} - d\frac{I_{LM1}}{n}\right] + \left[-\dot{d}\frac{\dot{i}_{LM2}}{n}\right]$$
(2.147)

$$C_B\left(\frac{dV_B}{dt} + \frac{dv_B}{dt}\right) = \left[\frac{I_{LM2}}{n} + I_0\right] + \left[\frac{i_{LM2}}{n} + i_0\right]$$
(2.148)

As previously done, the DC and second-order terms are neglected, thus yielding equations (2.149) and (2.150).

$$sC_{A}\dot{v_{A}}(s) = D'\frac{\dot{i_{LM1}}(s)}{n} - \dot{i_{0}}(s) - \dot{d}(s)\frac{I_{LM1}}{n}$$
(2.149)

$$sC_{B}\dot{v}_{B}(s) = \frac{\dot{i}_{LM2}(s)}{n} + \dot{i}_{0}(s)$$
 (2.150)

Isolating \hat{i}_{LM1} (s) in (2.143) and (2.149) result in (2.151) and (2.152), respectively.

$$\hat{i}_{LM1}(s) = \frac{\hat{d}(s)V_{IN}}{sL_{M1}} - D'\frac{v_A(s)}{sL_{M1}n} + \hat{d}(s)\frac{V_A}{sL_{M1}n}$$
(2.151)

$$\hat{i}_{LM1}(s) = \frac{\hat{i}_0(s)n}{D'} + \hat{d}(s)\frac{I_{LM1}}{D'} + \frac{sC_Av_A(s)n}{D'}$$
(2.152)

Substituting (2.151) into (2.152) yields (2.153).

$$\hat{v}_{A}(s) = \hat{d}(s) \left[\frac{\binom{V_{A}}{n} + V_{IN}}{D'^{2} + s^{2}L_{M}C_{o}n^{2}} - \frac{sL_{M}nI_{LM1}}{D'^{2} + s^{2}L_{M}C_{o}n} \right] - \hat{i}_{0}(s) \left[\frac{sL_{M}n^{2}}{D'^{2} + s^{2}L_{M}C_{o}n^{2}} \right]$$
(2.153)

Similarly, using (2.144) and (2.150) one can determine (2.154).

$$\hat{v}_{B}(s) = \hat{i}_{0}(s) \left[\frac{sL_{M}n^{2}}{1 + s^{2}L_{M}C_{o}n^{2}} \right]$$
(2.154)

Considering that $\hat{v}_{_0}(s) = \hat{v}_{_A}(s) - \hat{v}_{_B}(s)$, it is possible to derive (2.155).

$$\hat{v}_{0}(s) = \hat{d}(s) \left[\frac{\binom{V_{A}}{n} + V_{IN}}{D'^{2} + s^{2}L_{M}C_{o}n^{2}} - \frac{sL_{M}nI_{LM1}}{D'^{2} + s^{2}L_{M}C_{o}n} \right] - \hat{i}_{0}(s) \left[\frac{sL_{M}n^{2}}{D'^{2} + s^{2}L_{M}C_{o}n^{2}} \right] - \hat{i}_{0}(s) \left[\frac{sL_{M}n^{2}}{1 + s^{2}L_{M}C_{o}n^{2}} \right]$$

$$(2.155)$$

Finally, the output current to duty cycle small-signal transfer function is given by (2.156).

$$\hat{i_0(s)} = \frac{B_3 s^3 + B_2 s^2 + B_1 s + B_0}{A_4 s^4 + A_3 s^3 + A_2 s^2 + A_1 s + A_0}$$
(2.156)

Where:

$$B_{3} = -n^{3} L_{M}^{2} I_{LM} C$$

$$B_{2} = n^{2} (1-D) L_{M} C_{o} (V_{IN} n + V_{A})$$

$$B_{1} = -n L_{M} I_{LM}$$

$$B_{0} = (1-D) (V_{IN} n + V_{A})$$

$$A_{4} = n^{4} L_{M}^{2} C_{o}^{2} R_{o}$$

$$A_{3} = 2n^{4} L_{M}^{2} C_{o}$$

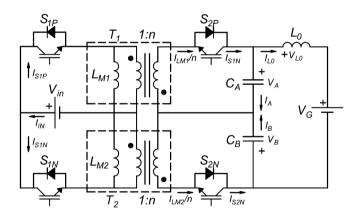
$$A_{2} = n^{2} R_{o} L_{M} C_{o} (D^{2} - 2D + 2)$$

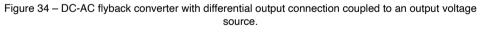
$$A_{1} = n^{2}L_{M} \left(D^{2} - 2D + 2 \right)$$
$$A_{0} = R_{o} \left(D^{2} - 2D + 1 \right)$$

3.10 Small-signal Analysis for the Alternative Switching Strategy Coupled to an Output Voltage Source

The small-signal analysis presented in section 2.3.9 considers the converter feeding a resistive output load. However, in order to operate connected to the utility line, the converter must be designed to operate injecting current into a voltage source. The coupling between the output filter of the converter with the voltage source is realized by adding L_0 to the circuit. Figure 34 presents the circuit of the converter for a designed for grid connection, where *VG* represents a given value of the utility grid voltage, which can be treated as constant within a switching cycle.

As mentioned in section 2.2.10, the output inductor L_o presented in Figure 34 acts toward limiting the ripple in the current injected in the voltage source V_{c} .





Source: Self-authorship

The analysis is performed by analyzing either the output voltage as $V_0>0$ or $V_0<0$. However, in accordance to the circuit presented in Figure 34, the analysis presented in this section consider the positive semi-cycle of the output voltage.

Similar to the circuit presented in Figure 27, the first operating stage of the converter connected to the utility line is presented in Figure 35. However, here the system has \hat{i}_{L0} as another state to be considered in the dynamic analysis. The mesh analysis of the voltage on L_0 gives a voltage value, in the first operating stage, as presented in equation (2.157).

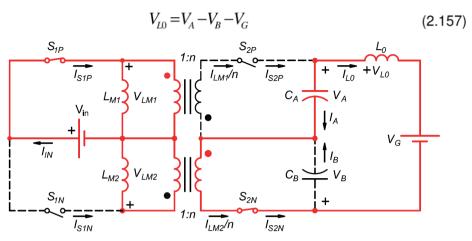


Figure 35 - 1st operating stage - alternative switching coupled to an output voltage source. Source: Self-authorship

Conveniently, the mesh analysis of the voltage on L_o during the second operating stage (Figure 36), presents the same sum of voltages described by equation (2.157).

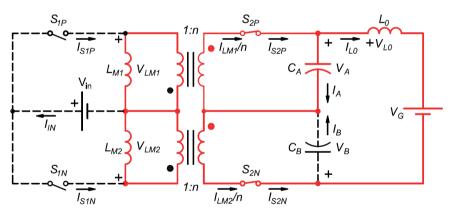


Figure 36 - 2nd operating stage - alternative switching coupled to an output voltage source. Source: Self-authorship

Therefore, the voltage balance of the L_a inductance is given by (2.158).

$$\langle v_{L0} \rangle = d(t) \langle v_A - v_B - v_G \rangle + d'(t) \langle v_A - v_B - v_G \rangle$$
(2.158)

Applying small perturbations in (2.158) results in (2.159), where the DC and secondorder terms and also variations of V_{g} were neglected.

$$L_0 \frac{d i_{L_0}}{dt} = \dot{v_A} - \dot{v_B}$$
(2.159)

The Laplace transform of the equation (2.159) returns (2.160).

$$sL_{0}\dot{i}_{LM}(s) = \dot{v}_{A}(s) + \dot{v}_{B}(s)$$
 (2.160)

The equations that define the voltage balance on both magnetizing inductances L_{M1} and L_{M2} , respectively presented in (2.137) and (2.138), remain the same. Therefore, their Laplace transforms are the same as well, as reintroduced, respectively, by equations (2.161) and (2.162).

$$sL_{M1}\hat{i}_{LM1}(s) = \hat{d}(s)V_{IN} - D\frac{v_A(s)}{n} + \hat{d}(s)\frac{V_A}{n}$$
(2.161)

$$sL_{M2}i_{LM2}(s) = -\frac{v_{B}(s)}{n}$$
 (2.162)

On the other hand, the current that defines the equations for the capacitors charge balance C_{A} and $C_{B'}$ respectively, in (2.145) and (2.146) changes from I_{o} to I_{Lo} . Thus, resulting in (2.163) and (2.164), respectively.

$$\langle i_{CA}(t) \rangle = d(t) \langle -i_{L0}(t) \rangle + d'(t) \langle \frac{i_{LM1}(t)}{n} - i_{L0}(t) \rangle$$
 (2.163)

$$\langle i_{CB}(t) \rangle = d(t) \left\langle \frac{i_{LM2}(t)}{n} + i_{L0}(t) \right\rangle + d'(t) \left\langle \frac{i_{LM2}(t)}{n} + i_{L0}(t) \right\rangle$$
 (2.164)

Proceeding similarly, one can derive (2.165) and (2.166) from (2.163) and (2.164), respectively.

$$sC_{A}\dot{v}_{A}(s) = D \frac{\dot{i}_{LM1}(s)}{n} - \dot{i}_{L0}(s) - \dot{d}(s) \frac{I_{LM1}}{n}$$
(2.165)

$$sC_{B}\dot{v_{B}}(s) = \frac{i_{LM2}(s)}{n} + i_{L0}(s)$$
 (2.166)

Overall, the small signal analysis of the converter connected to the utility line, presents five fundamental equations and five unknown variables, namely $\hat{i}_{LM1}(s)$, $\hat{i}_{LM2}(s)$, $v_{A}(s)$, $v_{B}(s)$, and $\hat{i}_{L0}(s)$, summarized in the system of equations presented in (2.167). It is considered in the analysis that $L_{M1}=L_{M2}=L_{M}$ and $C_{A}=C_{B}=C_{o}$.

$$\begin{cases} sL_{M} i_{LM1}(s) = d(s)E - D'v_{A}(s) + d(s)\frac{V_{A}}{n} \\ sL_{M} i_{LM2}(s) = -\frac{v_{B}(s)}{n} \\ sC_{o}v_{A}(s) = D'\frac{i_{LM1}}{n} - d(s)\frac{I_{LM1}}{n} - i_{L0}(s) \\ sC_{o}v_{B}(s) = i_{L0}(s) + \frac{i_{LM2}(s)}{n} \\ sL_{0}i_{L0}(s) = v_{A}(s) - v_{B}(s) \end{cases}$$
(2.167)

The desired control to output current transfer function is obtained by eliminating the unknown variables of the system of equations in (2.167), which returns the transfer function presented in (2.168).

$$\hat{i}_{L0}(s) = \frac{B_3 s^3 + B_2 s^2 + B_1 s + B_0}{A_5 s^5 + A_4 s^4 + A_3 s^3 + A_2 s^2 + A_1 s + A_0}$$
(2.168)

Where:

$$B_{3} = -C_{o}L_{M}^{2}n^{3}I_{LM1}$$

$$B_{2} = C_{o}L_{M}(1-D)n^{2}V_{A} + C_{o}L_{M}(1-D)n^{2}V_{IN}$$

$$B_{1} = -L_{M}nI_{LM1}$$

$$B_{0} = (1-D)V_{A} + (1-D)nV_{IN}$$

$$A_{5} = C_{o}^{2}L_{M}^{2}L_{0}n^{4}$$

$$A_{4} = 0$$

$$A_{3} = 2C_{o}L_{M}^{2}n^{4} + C_{o}L_{M}L_{0}(1-D)^{2}n^{2} + C_{o}L_{M}L_{0}n^{2}$$

$$A_{2} = 0$$

$$A_{1} = L_{M}(1-D)^{2}n^{2} + L_{M}n^{2} + L_{0}(1-D)^{2}$$

4 | CONCLUSION

It is presented in this chapter a dc-ac bidirectional converter with differential output connection and two switching strategies. The converter is a differential connection of two dc-dc bidirectional converters designed to operate in high- frequencies in order to generate a dc-ac high-frequency-isolated converter. The converter attends the initial proposal presented in Chapter 1, and subsequently introduced in section 2.1 of a single-stage high-frequency-isolated converter for grid connection.

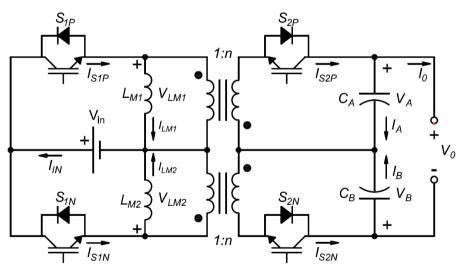
Two switching strategies are presented hereon. The first is the original switching strategy proposed by (CARDOSO, 2007), (CACERES e BARBI, 1999) and (CIMADOR e PRESTIFILIPPO, 1990), studied in depth. In addition, a new contribution is made in the control to output current transfer function of the converter connected to the utility grid. The second switching strategy has not been studied before and envisions improving the efficiency of the converter by means of reducing the RMS current of the switches in both windings of the flyback inductors. Also in this chapter, a transfer function of the duty-cycle-to-output-current for a linear load and another that presents the converter connected to the utility grid has been presented. All currents and voltages for all components of the circuit are studied in depth for both switching strategies.

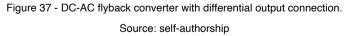
DESIGN, SIMULATION AND EXPERIMENTAL RESULTS OF A DC-AC FLYBACK CONVERTER

1 | INTRODUCTION

This chapter presents the project of the converter analyzed in Chapter 2. First, a design methodology is proposed in order to determine and satisfy the design requirements. Initial calculations based on the requirements shows that a single converter is able to handle both switching strategies. This procedure allows a fair comparison between both switching strategies as well as the authentication of the alternative switching strategy's advantages. The calculated values in the design methodology are confirmed by means of numerical simulation and put into comparison for choice of components. Finally, experimental results are shown for open-loop operation and some considerations towards the dynamics of the converter are made.

Figure 37 presents the sign conventions for voltages and currents adopted for the design of the dc-ac flyback converter.





2 I DESIGN METHODOLOGY

The design methodology starts with the presentation of the requirements in Table 3, which are carried from one modulation to another, considering that the original intent is to share the same prototype.

Input Voltage	E [V]
RMS Output Voltage	V _{orms} [V]
Active Output Power	P _。 [W]
Switch Frequency	f _s [Hz]
Coupled Inductor Current Ripple	Δ _{ι_} [%]
Output Voltage Ripple	Δ _{νο} [%]
Coupled Inductor Turns Ratio	п

Table 3 - List of project requirements.

Source: Self-authorship

Once the requirements are known, one can follow the steps of the scrip below to design the converter.

- · Determine the peak output voltage;
- · Calculate the duty cycle to obtain the required peak output voltage;
- Calculate the magnetizing inductance based on the values for peak output power;
- Calculate the output capacitance C_A and C_B ;
- Calculate the maximum voltage over C_A and C_B ;
- Calculate the average and RMS current values and the maximum voltage for the semiconductors.

3 | REQUIREMENTS SPECIFICATIONS

Considering that the main goal of this thesis to design single-stage high- frequencyisolated inverters for power grid connection, it has been chosen a small wind turbine simulator available at the laboratory of the Federal University of Technology of Paraná as power supply. An algorithm designed to simulate the behavior of a wind turbine controls the motor-generator setup that generates a rectified *70Vdc* when its speed is set for maximum speed. The requirements of output voltage (*127 VAC*) and grid frequency (*60 Hz*) of the converter were adopted to match the voltage standard of the Paraná state in Brazil.

Initially, a *1kW* output power was considered, but further investigation revealed that such output power would lead to low efficiency, due to switching and conduction losses. In order to work with lower current levels, an output power of *500 W* was adopted. This decision allowed the converter to operate lower current levels, which ultimately lead to lower magnetizing inductances; therefore, a possible reduction in the leakage inductance.

As well as the output power, the switching frequency had to be reduced once the switching losses were calculated. Initially stipulated as *100 kHz*, concerns about the driver technology that would be used and switching losses that could potentially degrade the overall efficiency of the converter, led to the decision of reducing the switching frequency to *20 kHz*. In addition, a potential high leakage inductance could do devastating damage to the converter in higher switching frequencies.

As seen in equations (2.8) and (2.109), the higher the current ripple becomes, the lower the magnetizing inductance is. The same can be said about the switching frequency, where higher switching frequencies results in lower magnetizing inductances. Therefore, because of the switching frequency adjustment from *100 kHz* to *20 kHz*, a large current ripple had to be adopted for the coupled inductor. This allowed the converter to operate with smaller magnetizing inductances.

The turns ratio of the flyback inductor were defined as n=1 in order to observe the same current efforts in all four switches and to reduce a potential issue caused by parasite and leakage inductances. This was considered an interesting point, where the best semiconductor technology is, by date, rated for voltage levels below 600V. On the other hand, there is the considerable disadvantage of not using the turns ratio of the coupled inductor as a way to boost the output voltage. Thus, the voltage conversion ratio of the converter relies solely on the duty cycle of the converter, as predicted in equations (2.3) and (2.100). Another limiting factor is that, the prototype had to be designed to operate with both switching strategies and perform with satisfactory efficiency levels for the purpose of comparison, which means that this requirement is not optimized for none of the switching strategies.

Table 4 summarizes the requirements adopted for the design of the dc-ac flyback converter with differential output connection.

Input Voltage	Е	70 V
RMS Output Voltage	V _{o_RMS}	127 V
Output Voltage Frequency	f _r	60 Hz
Active Output Power	P _o	500 W
Switching Frequency	f _s	20 kHz
Coupled Inductor Current Ripple	Δ_{l_L}	50 %
Coupled Inductor Turns Ratio	n	1

Table 4 – DC-AC flyback w/ differential output connection - requirements specifications.

Source: Self-authorship

Despite the active output power presented in Table 4 is *500 W*, the maximum power processed by each semi-cycle is twice the desired average output power. Therefore, the actual active output power considered to calculate the values presented in Table 5 is *1 kW*, which corresponds to the power processed when $a = \pi/2$ and $a = 3\pi/2$.

4 | NUMERICAL SIMULATION

This section presents the simulation results obtained for the complementary and alternative switching methods. The value of the components used for both simulations are presented in Table 5 and were calculated based on the requirements presented in Table 4. The calculations presented for the complementary switching strategy are presented in Appendix A, while the calculations for the alternative switching strategy are presented in Appendix B.

The values presented in Table 5 confirms that the alternative switching strategy has the advantages of operating the same output power with smaller duty cycle and reduced RMS current in all four switches (i.e. S_{1P} , S_{2P} , S_{1N} and S_{2N}), although the magnetizing inductance calculated is higher for the alternative switching strategy.

	Complementary SW ¹	Alternative SW ²	Difference (Comp/Alt)
Maximum Output Voltage	179.6 V	179.6 V	
Maximum Duty Cycle	0.744	0.72	3.33 %
Magnetizing Inductance	239.328 <i>µ</i> H	253.704 μH	-5.66 %
Mag. Inductance Current	21.767 A	19.853 A	9.64 %
Output Capacitors	3.974 μF	4.1 <i>µ</i> F	
Capacitors Max. Voltage	221.176 V	179.6 V	23.14 %
Average Current ($S_{\eta P}$)	3.571 A	3.571 A	0 %
RMS Current (S_{1P})	8.941 A	7.548 A	18.45 %
Max. Voltage ($S_{\gamma P}$)	273.664 V	249.605 V	9.638 %
Average Current (S_{1N})	3.571 A	3.571 A	
RMS Current (S_{1N})	8.941 A	7.548 A	18.45 %
Max. Voltage (S_{1N})	273.664 V	249.605 V	9.638 %
Average Current (S_{2P})	0 A	0 A	
RMS Current (S_{2P})	6.636 A	5.777 A	14.86 %
Max. Voltage (S_{2P})	273.664 V	249.605 V	9.638 %
Average Current (S_{2P})	0 A	0 A	

1 Calculations presented in Appendix A

2 Calculations presented in Appendix B

RMS Current (S_{2P})	6.363 A	5.777 A	14.86 %
Max. Voltage (S_{2P})	273.664 V	249.605 V	9.638 %

Table 5 – DC-AC flyback w/ differential output connection - calculated values.

Source: Self-authorship

4.1 Complementary Switching Strategy

The simulated circuit for the complementary switching strategy is presented in Figure 38. All simulations were performed by power electronics simulation software PSIM®.

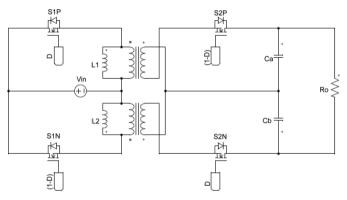


Figure 38 - Simulation circuit - complementary SW Source: self-authorship

Figure 39 presents the simulation results for the output voltage of the converter and its FFT analysis. It is noticeable that the converter almost produces no additional harmonic content in open-loop without any duty cycle linearization.

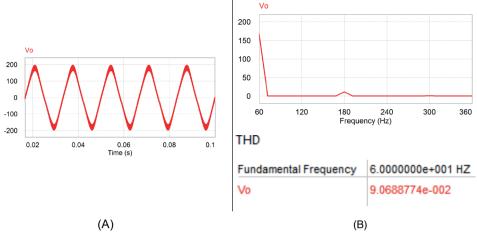
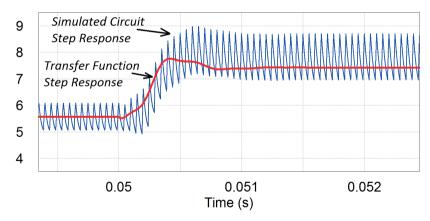
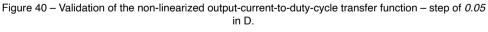


Figure 39 - Non-linearized output voltage. (A) V_{o} (B) FFT / THD. Source: self-authorship

Figure 40 presents the step response of the non-linearized control to output current transfer function presented in section 2.2.9. The duty cycle step given to obtain the result presented was of D=0.05, which elevates the original duty cycle of D=0.744 to D=0.794.





Source: self-authorship

For smaller duty cycle variations, the non-linearized transfer function presents more accurate response, as presented in Figure 41 for a duty cycle variation of D=0.02.

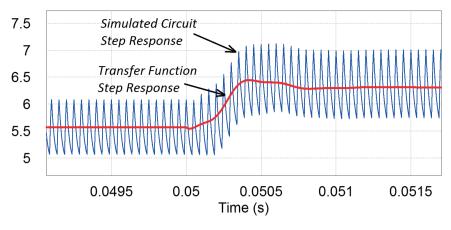


Figure 41 – Validation of the non-linearized output current to duty cycle transfer function - step of 0.02 in D.

Source: self-authorship

The duty cycle of the converter can be linearized, using the equation presented in (2.4) for a given voltage conversion ratio. For the requirements given in Table 4, the voltage conversion ratio, as presented in (2.169), is *2.566*.

$$q = \frac{V_0}{En} = \frac{179.6}{70 \times 1} = 2.566$$
(2.169)

The linearized duty cycle of the converter presents a waveform of the output voltage even more similar to a sinusoidal waveform, which reduces the already low harmonic content, as presented by Figure 42 (B). Figure 42 (A) shows the simulation result of the output voltage with the duty cycle linearized, using the equation given by (2.170).

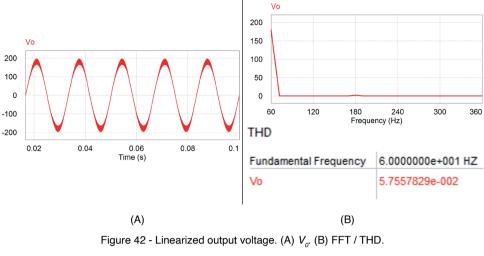
$$D(\alpha) = \frac{q(\alpha) - 2n + \sqrt{q(\alpha)^2 + 4n^2}}{2q(\alpha)}$$
(2.170)

The small signal linearized duty cycle of the converter is defined as the partial derivative of (2.170), given by (2.171).

$$\hat{d} = \frac{\partial D}{\partial q} \hat{q}$$
(2.171)

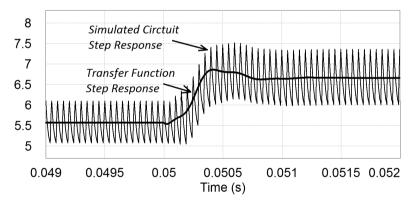
Substituting (2.170) into (2.171), results in (2.172).

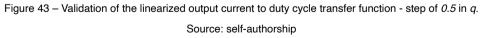
$$\hat{d} = \left[\frac{-2 + \sqrt{q^2 + 4}}{q^2 \sqrt{q^2 + 4}}\right] \hat{q}$$
(2.172)



Source: self-authorship

Therefore, for a given voltage conversion ratio, equation (2.172) returns the equivalent small signal variation of the duty cycle. The comparative response for a voltage conversion ratio of the linearized control to output current transfer function with the simulated circuit (Figure 38) is presented in Figure 43. The step given was of q=0.5.





Because of the superior results presented with the linearization of the duty cycle, the following waveforms presented hereon are waveforms of the converter operating with the linearization of the duty cycle by the angular variation of the voltage conversion ratio presented in (2.170).

Figure 44 shows the PWM pulses of the complementary switching method for each resultant output voltage (V_{o}).

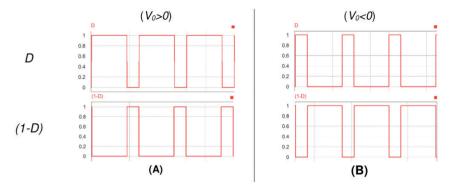


Figure 44 – PWM command for (A) Positive semi-cycle ($V_{o}>0$). (B) Negative semi-cycle ($V_{o}>0$). Source: self-authorship

Figure 45 presents the waveforms of the currents in all four switches for both semicycles of the output voltage. The similarity of the simulated waveforms and the theoretical (see Figure 16) confirms the assumptions made to obtain the equations presented in Chapter 2.

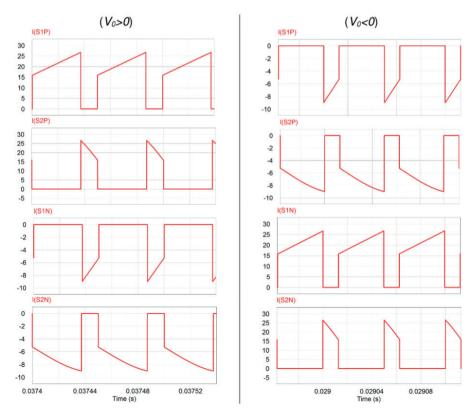


Figure 45 - Simulated current waveforms in all four switches - complementary switching strategy. Source: self-authorship

The maximum voltages for switches $S_{_{1P}}$ and $S_{_{2P}}$ are registered for V_o >0 when $a=\pi/2$. Figure 46 presents the waveforms of the voltage variation over switches $S_{_{1P}}$ and $S_{_{2P}}$. These waveforms confirm the theoretical waveforms in Figure 16.

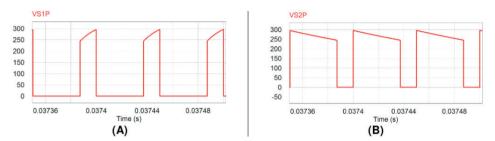


Figure 46 – Simulated voltages waveforms for $V_{_{0}}$ >0 in (A) $S_{_{1P}}$ (B) $S_{_{2P}}$ - Complementary switching strategy.

Source: self-authorship

Similarly, the maximum voltages over switches S_{1N} and S_{2N} are registered for $V_0 < 0$ when a = $3\pi/2$. Figure 47 presents the waveforms of the voltages over switches S_{1N} and S_{2N} for a maximum output voltage in the negative semi-cycle.

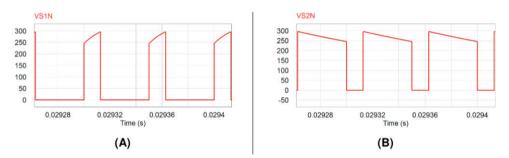


Figure 47 - Simulated waveforms for V_{σ} >0 in (A) $S_{_{1N}}$ (B) $S_{_{2N}}$ - Complementary switching strategy. Source: self-authorship

Table 6 presents the comparison of all the calculated values (using the proposed design methodology in section 3.2) with the results obtained via numerical simulation. These results were judged accurate enough to validate the calculations presented and for the purpose of comparison.

Varia	able	Calculated ³	Simulated	Difference (Calc./Sim.)
RMS Output Voltage	Vo_RMS	127 V	125.9 V	0.88 %
Peak Output Voltage	$Vpk_POS(\pi/2) + \Delta V_0/2$	203.664 V	196.7 V	3.55 %
Avg. Output Current	l ₀ (π/2)	5.568 A	5.516 A	0.95 %
Input Current	l _e (π/2)	14.286 A	14.086 A	1.42 %
Mag. Inductance Current	I∟(<i>π</i> /2)	21.767 A	21.387 A	1.78 %
Peak Current (S _{1P})	IS _{1P} _max(<i>n</i> /2)	27.209 A	26.791 A	1.57 %
Average Current ($S_{_{1P}}$)	$IS_{_{1P}}(0{\rightarrow}2\pi)$	3.571 A	3.507 A	1.83 %
RMS Current ($S_{_{1P}}$)	$IS_{1P-}RMS (0 \rightarrow 2\pi)$	8.941 A	8.747 A	2.22 %
Max. Voltage ($S_{_{1P}}$)	VS _{1P} (π/2)	291.176 V	296.21 V	-1.69 %
Peak Current ($S_{_{1P}}$)	IS _{1N} _max(3π/2)	27.209 A	26.795 A	1.55 %
Average Current ($S_{_{IN}}$)	IS _{1N} (0→2π)	3.571 A	3.508 A	1.8 %
RMS Current ($S_{_{1N}}$)	$IS_{1N-}RMS (0 \rightarrow 2\pi)$	8.941 A	8.75 A	2.19 %
Max. Voltage ($S_{_{1N}}$)	VS _{1N} (3 <i>n</i> /2)	291.176 V	296.21 V	-1.69 %
Peak Current ($S_{_{2P}}$)	IS _{2P} _max(π/2)	27.209 A	26.773 A	1.63 %
RMS Current ($S_{_{2P}}$)	$IS_{2P}RMS (0 \rightarrow 2\pi)$	6.363 A	6.308 A	0.88 %
Max. Voltage ($S_{_{2P}}$)	VS _{2P} (<i>1</i> /2)	291.176 V	296.18 V	-1.68 %
Peak Current ($S_{_{2N}}$)	IS _{2N} _max(3π/2)	27.209 A	26.795 A	1.55 %
RMS Current ($S_{_{2N}}$)	$IS_{2N-}RMS (0 \rightarrow 2\pi)$	6.363 A	6.308 A	0.88 %
Max. Voltage ($S_{_{2N}}$)	VS _{2N} (3π/2)	291.176 V	296.21 V	-1.69 %

Table 6 - Complementary SW - comparison of results.

Source: Self-authorship

For the analysis of the transfer function of the converter coupled to an output voltage source, it is necessary to understand that system described by the transfer function acts like an integrator. This characteristic is given by the term A_o in (2.99), which is always equal to zero. Therefore, when the transfer function is submitted to a step in the duty cycle, the response is integrated for infinity, as presented in Figure 48.

³ Calculations presented in Appendix A

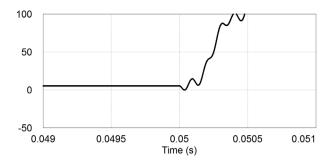


Figure 48 – Complementary switching strategy – open loop step response of the transfer function of the converter coupled to an output voltage source.

Source: self-authorship

This response is an indication that the converter cannot operate connected to the utility grid in open loop. Therefore, in order to validate this transfer function, a simple PI controller, designed for the sole purpose of stabilizing the output was designed and simulated. The response of the converter and the transfer function in this simulation are presented in Figure 49.

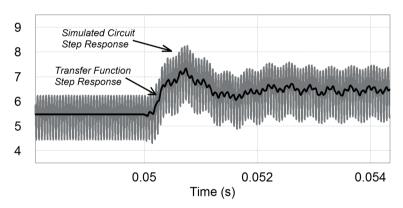


Figure 49 – Complementary switching strategy – closed loop step response of the transfer function of the converter coupled to an output voltage source.

Source: self-authorship

In this case, the small-signal duty cycle $\hat{d}(s)$ has to be taken from the output of the controller, which is made by subtracting the duty cycle of the steady-state operation when the step is applied, leaving only the small variations of the duty cycle. This operation is depicted in Figure 50, where: ref is the current reference; step(ts) is the current step given in ts; C(s) is the controller; D/d is the operation performed; G(s) is the plant of the converter; DC(s) is the duty cycle as an output of the controller C(s); and Dst is the steady-state duty-cycle before the step.

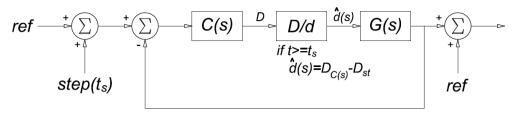
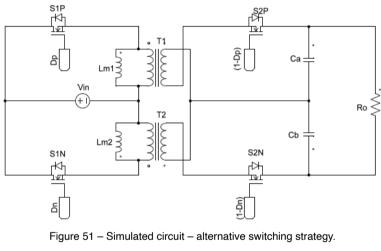


Figure 50 – Complementary switching strategy – small-signal duty cycle operation. Source: self-authorship

4.2 Alternative Switching Strategy

The simulated circuit of the converter operating with its alternative switching strategy is presented in Figure 51.



Source: self-authorship

Figure 52 presents the output voltage of the converter and its FFT analysis. Through simulation it is noticeable that the alternative switching strategy presents higher harmonic content than the complementary switching strategy (Figure 39) in the third, fifth and seventh harmonics.

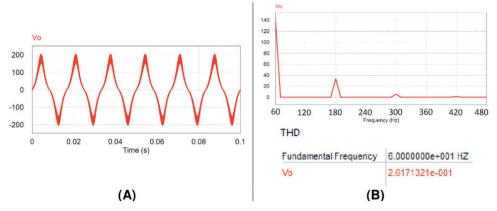
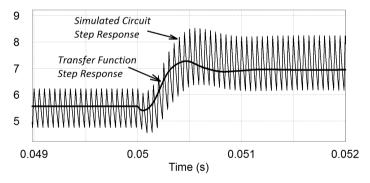
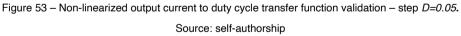


Figure 52 – Non-linearized output voltage (A) V_{σ} (B) FFT / THD. Alternative switching strategy. Source: self-authorship

The open loop transfer function of the alternative switching strategy is presented in Figure 53. The step response of the duty cycle to output current transfer function presents a better response, in terms of transitory behavior. In Figure 53 the difference of the average output current is *96 mA* before the step and *208 mA* after the step in the duty cycle.





The duty cycle of the converter can be linearized in order to reduce the low frequency harmonics and correct the waveform of the output voltage to a sinusoidal form. As described for the complementary switching strategy, the duty cycle of the converter can be linearized for a given voltage conversion ratio *q*. Considering that the requirements for both switching strategies are the same, the value for *q=2.566* described in (2.169) is valid for the alternative switching strategy as well. The duty cycle of the converter for any given angle of a is presented in (2.103) for switches S_{1P} and S_{2P} and in (2.104) for switches S_{1N} and S_{2N} . The simulation result of the output voltage obtained from the linearization of the duty cycle is

presented in Figure 54.

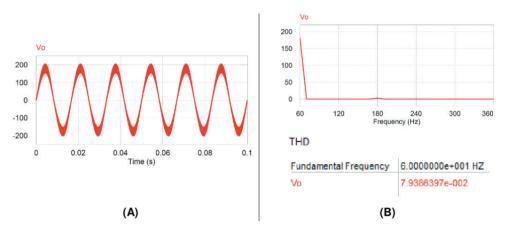


Figure 54 – Linearized output voltage (A) V_o (B) FFT. Alternative switching strategy. Source: self-authorship

In comparison to the results presented in Figure 52, the simulated output voltage in Figure 54 presents a waveform that best resembles a sinusoidal waveform, which can be confirmed by the reduction of the harmonics in Figure 54 (B).

The linearization of the small-signal variations of the duty cycle \hat{d} is obtained by the partial derivative of equation (2.101) as presented in (2.171), which results in (2.173).

$$\hat{d} = \left[\frac{V_{IN}^{2}}{\left(V_{A}n - V_{B}n + V_{IN}\right)^{2}}\right]\hat{q}$$
(2.173)

Therefore, for a given voltage conversion ratio q, (2.173) returns the equivalent duty cycle. Figure 55 presents a comparative response of the simulated circuit with the duty cycle to output current transfer function from a step of q=0.5. The difference before the step between the circuit and the transfer function is 96 mA and after the step is given, when the current settles, the difference goes to 109 mA.

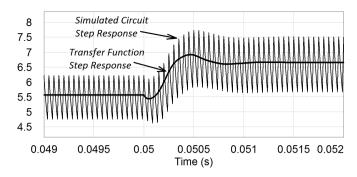


Figure 55 – Linearized output-current-to-duty-cycle transfer function validation – step of 0.5 in q. Source: self-authorship

Because the results were better with the linearization function, the results presented in this section are exclusive to this condition.

Figure 56 shows the PWM pulses for all four switches in the simulated circuit and the equivalent response of the output voltage. It is noticeable that, in order to use the same output capacitors (C_A and C_B) in the converter, the output voltage ripple is bigger than the voltage ripple registered for the complementary switching strategy. This is due to the equation of the capacitor being dependent on the duty cycle and the duty cycle (for the same voltage conversion ratio) being lower in the alternative switching strategy. Under these circumstances, the output voltage varies from 1153 VI to 1201.4 VI, registering a variation of 148.35 VI in both semi-cycles, as depicted in Figure 56.

The output voltage ripple considered for the alternative switching strategy is $\Delta V_0 =$ 28% while in the complementary it is 19.5%.

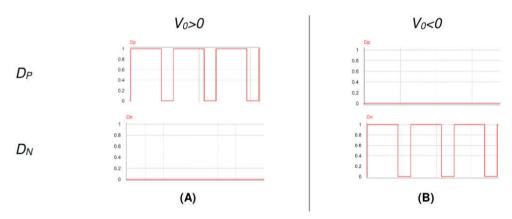


Figure 56 – PWM command for (A) positive semi-cycle ($V_o > 0$). (B) Negative Semi-cycle ($V_o > 0$). Source: self-authorship

Figure 57 presents the waveforms of the currents in all four switches for the positive semi-cycle (A) and for the negative semi-cycle (B), both when the output voltage reaches its maximum. It confirms the theoretical waveforms presented to derive the equations for the current in the switches in section 2.2 Figure 16.

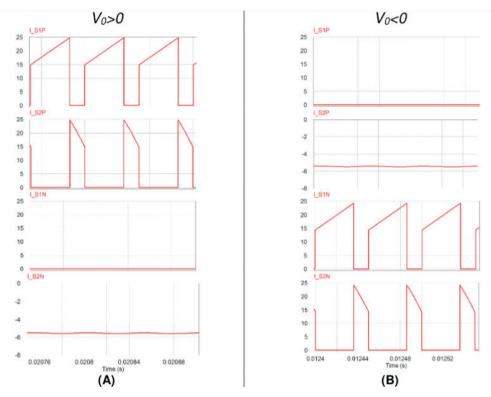


Figure 57 – Simulated current waveforms in all four switches – complementary switching strategy. (A) Positive Semi-cycle. (B) Negative Semi-cycle.

Source: self-authorship

Figure 58 shows the current in the magnetizing inductances, which proves that the alternative switching strategy operates in the continuous conduction mode (CCM) in both positive and negative semi-cycle.

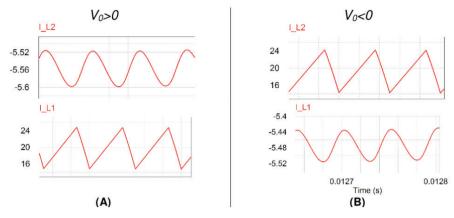


Figure 58 – Alternative switching strategy – simulated current waveforms of the magnetizing inductances (A) V_{o} >0. (B) V_{o} >0.

Source: self-authorship

Variable		Calculated ⁴	Simulated	Diff. (%)
RMS Output Voltage	V _{o_RMS}	127 V	125.8 V	0.96 %
Peak Output Voltage	$V_{pk_{POS(NEG)}} + \Delta V_0/2$	204.03 V	204.93 V	0.43 %
Quasi-Inst. Output Current	Ι _。 (π/2)	5.568 A	5.547 A	0.38 %
Input Current	l _e	14.28 A	14.24 A	0.29 %
Mag. Inductance Current	Ι_ (π/2)	19.85 A	19.81 A	0.21 %
Cap. Peak Voltage	V _a (π/2) / V _b (3π/2)	179.6 V	179.2 V	0.23 %
Peak Current (S _{1P})	Ι (π/2)	24.81 A	24.8 A	0.05 %
Average Current (S_{1P})	I _{S1P}	3.51 A	3.45 A	1.74 %
RMS Current (S_{1P})	l s1P_RMS	7.54 A	7.52 A	0.27 %
Max. Voltage (S_{1P})	V(π/2)	274.03 V	271.11 V	1.08 %
Peak Current (S_{1P})	Ι _{S1N_max} (3π/2)	24.81 A	24.26 A	2.27 %
Average Current ($S_{_{1N}}$)	I _{S1N}	3.51 A	3.55 A	1.12 %
RMS Current (S_{1N})	l _{s1n_rms}	7.54 A	7.32 A	3.01 %
Max. Voltage $(S_{_{1N}})$	V _{S1N} (3π/2)	274.03 V	270.96 V	1.14 %
Peak Current (S_{2P})	Ι (π/2)	24.81 A	24.76 A	0.21 %
RMS Current (S_{2P})	I S2P_RMS	5.77 A	5.76 A	0.18 %
Max. Voltage ($S_{_{2P}}$)	V _{S2P} (π/2)	274.03 V	270.96 V	1.14 %
Peak Current (S_{2N})	I _{S2N_max} (3π/2)	24.81 A	24.26 A	2.27 %
RMS Current (S_{2N})	I S2N_RMS	5.77 A	5.69 A	1.41 %
Max. Voltage (S_{2N})	V_ _{S2N} (3π/2)	274.03 V	271.11 V	1.08 %

Table 7 - Alternative SW - comparison of results.

Source: Self-authorship

⁴ Calculations presented in Appendix B

The transfer function of the converter coupled to an output voltage source is validated the same way it is for the complementary switching strategy. Similarly, in the alternative switching strategy the system acts like an integrator, which makes the converter instable for open loop operation. Figure 59 shows the step response of the transfer function.

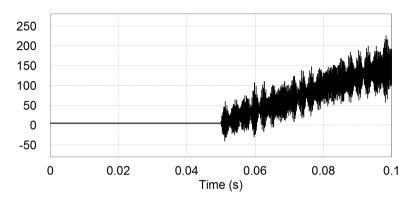


Figure 59 – Alternative switching strategy – open loop response of the transfer function of the converter coupled to an output voltage source.

Source: self-authorship

Because A_0 is zero in (2.168), the step response of the converter in open-loop tends to infinity. Therefore, as proposed for the complementary switching strategy, the step response of the transfer function is stabilized using a controller.

A PI controller was designed to generate the step response presented in Figure 60, where the response of the circuit is compared to the response of the transfer function. From this comparison, it is possible to conclude that the response of the transfer function predicts with good fidelity the behavior of the converter.

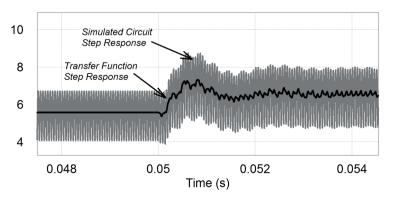


Figure 60 – Alternative switching strategy – closed loop response of the transfer function of the converter coupled to an output voltage source.

Source: self-authorship

For controlling and extracting the small signal variation of the duty cycle, the same scheme proposed in Figure 50 was used.

4.3 Comparison of Simulation Results

The simulation results presented for the complementary and alternative switching strategies, respectively, in Table 6 and Table 7 demonstrate relative accuracy with the calculated values. The average difference of the values displayed in both tables are 2%. Therefore, considering this proximity between calculated and simulated parameters, Table 8 presents the difference of the results obtained by means of simulation between both switching strategies. This comparison confirms the prerogative of the alternative switching strategy of decreasing the RMS current values in the semiconductors of the circuit.

Varia	able	Complementary	Alternative	Diff. (%)
RMS Output Voltage	V _{o_RMS}	125.9 V	125.8 V	0.08 %
Peak Output Voltage	$V_{_{pk_{-}POS}}(\pi/2) + \Delta V_{_{o}}/2$	196.7 V	204.93 V	4.01 %
Avg. Output Current	Ι _。 (π/2)	5.516 A	5.547 A	0.55 %
Input Current	l _e (π/2)	14.086 A	14.24 A	1.08 %
Mag. Inductance Current	I_ (π/2)	21.387 A	19.81 A	7.97 %
Peak Current (S _{1P})	I _{S1P_max} (π/2)	26.791 A	24.8 A	8.03 %
Average Current (S_{1P})	I _{S1P} (0→2π)	3.507 A	3.45 A	1.66 %
RMS Current (S_{1P})	I _{S1P_RMS} (0→2π)	8.747 A	7.52 A	16.32 %
Max. Voltage (S_{1P})	V _{S1P} (π/2)	296.21 V	271.11 V	9.26 %
Peak Current (S_{1P})	I _{S1N_max} (3π/2)	26.795 A	24.26 A	10.45 %
Average Current (S_{N})	I _{s1N} (0→2π)	3.508 A	3.55 A	1.18 %
RMS Current (S _{1N})	I _{S1N_RMS} (0→2π)	8.75 A	7.32 A	19.54 %
Max. Voltage ($S_{_{1N}}$)	V _{s1N} (3π/2)	296.21 V	270.96 V	9.32 %
Peak Current (S_{2P})	I _{S2P_max} (π/2)	26.773 A	24.76 A	8.14 %
RMS Current (S_{2P})	I _{S2P_RMS} (0→2π)	6.308 A	5.76 A	9.52 %
Max. Voltage ($S_{_{2P}}$)	V_ _{S2P} (π/2)	296.18 V	270.96 V	9.31 %
Peak Current (S_{2N})	Ι (3π/2)	26.795 A	24.26 A	10.45 %
RMS Current (S_{2N})	I _{S2N_RMS} (0→2π)	6.308 A	5.69 A	10.87 %
Max. Voltage (S_{2N})	V_ _{S2N} (3π/2)	296.21 V	271.11 V	9.26 %
Non-linearized THD	THD	0.09 %	0.26 %	

Table 8 – Comparison of simulation results.

Source: Self-authorship

5 | CHOICE OF COMPONENTS AND PROTOTYPE BUILT

Based on calculations and simulation results, this section highlights the main requirements adopted to choose the components for the prototype. It also presents the

requirements adopted to make the flyback inductors and the winding procedure adopted.

5.1 Switches

The first requirement observed to choose the switches were the maximum voltages and currents during steady-state operation. According to the calculations, both maximum voltage and current values are registered for the complementary switching strategy, as presented in Table 9. As already mentioned in section 3.3, each semi-cycle has to process 1 kW in order to average an output power of *500 W*. Therefore, all calculated values presented are for 1 kW.

The maximum current considered is *27.209 A* and the maximum voltage is *299.707 V*. Based on these values, the semiconductor chosen for this application was the Infineon IKW40N65F5. Table 10 displays the main characteristics of this IGBT.

	Variable	Complementary Switching⁵	Alternative Switching ⁶
	V _{S1P_max}	299.707 V	274.031 V
Max. Voltage	V V ^{S2P_max} V _{S1N_max}	299.707 V 299.707 V	274.031 V 274.031 V
	V _{S2N_max}	299.707 V	274.031 V
	I S1P_max	27.209 A	24.817 A
Peak	l S2P_max	27.209 A	24.817 A
Current	 S1N_max	27.209 A	24.817 A
	l _{S2N_max}	27.209 A	24.817 A
	I /I S1P / I S1P_RMS	3.571 A / 8.941 A	3.571 A / 7.548 A
Average / RMS	I _{S2P} / I _{S2P_RMS}	0 A / 6.363 A	0 A / 5.777 A
Current	I / I S1N S1N_RMS	3.571 A / 8.941 A	3.571 A / 7.548 A
	I /I _{S1N} /I _{S2N_RMS}	0 A / 6.363 A	0 A / 5.777 A

Table 9 - DC-AC flyback converter with differential output connection – requirements for choice of switches.

Source: Self-authorship

An estimative of switching and conduction losses for this IGBT is presented in Appendix C for the complementary switching strategy and in Appendix E for the alternative switching strategy. According to the calculations, between switching and conduction losses, a grand total of *16.278 W* is expected to be dissipated during the operation of the converter in rated output power.

⁵ The values displayed in Table 9 for the complementary switching strategy are available on Appendix A.

⁶ The values displayed in Table 9 for the alternative switching strategy are available on Appendix B.

	Variable	Datasheet Value
Maximum Voltage	V _{CE}	650 V
DC Collector Current	$I_{c} = 25^{\circ}C$ $I_{c} = 100^{\circ}C$	74 A 46 A
Pulsed Collector Current	l _{Cpuls}	120 A
Threshold Voltage	V _{TH}	1.25 V

Table 10 - IGBT IKW40N65F5 main characteristics.

Source: Self-authorship

5.2 Output Filter Capacitors

In this converter, because of the AC output of the converter, it is not possible to use electrolytic capacitors. Therefore, a reliable capacitor for these applications is the polypropylene capacitor. Based on the calculations presented in Table 6 and Table 7, the rated voltage for these capacitors should be no smaller than *300 V*. The capacitors chosen for the application was the polypropylene capacitor VISHAY MKP 1840-1 and generic *1* μ F/400 *V* polyester capacitors. Table 11 shows the details of the MKP 1840-1 capacitor.

	Variable	Datasheet Value
Capacitance	С	1 <i>µ</i> F
Rated Voltage	U _R	400 V
Permissible AC Voltage	U _{R_RMS}	250 V

Table 11 - Capacitor VISHAY MKP1840.

Source: Self-authorship

5.3 Flyback Inductor

Table 12 presents the requirements from both switching strategies to build the flyback inductor.

Variable	Complementary	Alternative
L _{M1} / L _{M2}	239.328 µH	253.715 μH
IS1P_max	27.209 A	24.817 A
 S1N_max S2P_max	27.209 A 27.209 A	24.817 A 24.817 A
 S2P_max	27.209 A	24.817 A
I S1P_RMS	8.941 A	7.548 A
l _{S1N_RMS}	8.941 A	7.548 A
 S2P_RMS	6.363 A	5.777 A
 S2P_RMS	6.363 A	5.777 A
$\Delta I_{_{LM}}$	10.884 A	9.927 A
n	1	1
f _s	20k Hz	20k Hz
	L_{M1} / L_{M2} I_{S1P_max} I_{S1P_max} I_{S2P_max} I_{S2P_max} I_{S1P_RMS} I_{S1P_RMS} I_{S2P_RMS} I_{S2P_RMS} ΔI_{LM} n	$\begin{array}{c c c c c c c c c c c c c c c c c c c $

Table 12 - Flyback inductor requirements.

Source: Self-authorship

Because of the higher inductance value, the flyback inductor was designed by the requirements of the alternative switching strategy, with a margin in the current to support the higher current of the complementary switching strategy. The whole design of the flyback inductor and its losses are presented in Appendix C.

The winding technique adopted consists in winding half of each winding interchangeably in order to increase the practical coupling factor. Figure 61 illustrates the winding technique used to build the flyback inductor.

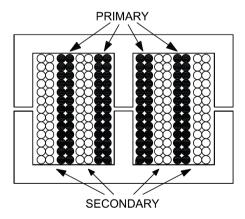


Figure 61 – DC-AC Flyback converter with differential output connection - winding technique adopted for the construction of the flyback inductor.

Source: Self-authorship

5.4 Clamp Circuit

To minimize the effects of hard switching, an RCD clamp is employed for each switch, as presented in the schematic of Figure 62. Considering that the maximum voltage on each switch is supposedly the same, as Table 9 indicates, the same diodes and resistors were initially applied for each switch.

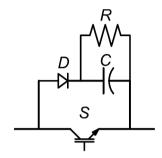


Figure 62 - RCD clamp. Source: Self-authorship

It has been decided that the RCD clamp resistance would be adjusted throughout the initial tests, in order to combine converter performance and clamping voltage. As the experimental test were performed, the resistance of two 5 W 56 k Ω in series proved to be the best solution for the allowable rated voltage of the switch that would less impact the efficiency of the converter.

The clamp capacitors were specified to support the calculated voltage over the switches of a maximum of 307.5 V. Therefore, the capacitors used in the clamp circuit of $S_{_{1P}}$ and $S_{_{1N}}$ were polyester capacitors of 1 μ F / 400 V. On the other hand, in the secondary (clamp circuit of $S_{_{2P}}$ and $S_{_{2N}}$) it has been chosen polyester capacitors of 470 η F / 400 V. In the primary, the higher capacitance values are justified by the higher RMS current of the switches.

The diodes chosen are the MUR460, whose average rectified current is 4 A, the peak reverse voltage is 600 V and the maximum instantaneous forward voltage is 1.05 V at 1500 C.

5.5 Prototype

Figure 63 presents the picture of the prototype built under the specifications presented in the previous sections of this chapter.

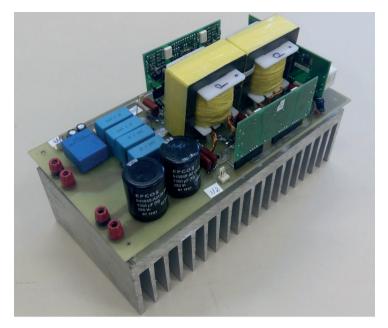


Figure 63 – DC-AC flyback converter with differential output connection – prototype. Source: Self-authorship

The test setup comprises of the following equipment:

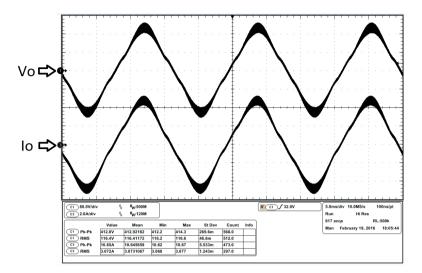
- Texas Instruments TMS320F28335 DSP: Used to generate the command pulses for the IGBTs;
- Tektronix DP0754C oscilloscope: all waveforms and THD measurements presented;
- · Yokogawa WT500 power meter: all efficiency measurements.

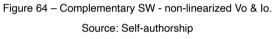
6 | EXPERIMENTAL RESULTS

This section presents the open loop experimental results for both modulation strategies. Initially, it shows the prototype operating the complementary switching strategy. The linearized and non-linearized output are presented with a resistive load. Next the linearized duty cycle is tested for nonlinear loads. The same experiments are made for the alternative switching strategy. Finally, the efficiencies of both switching strategies are compared for both linear and nonlinear loads.

6.1 Complementary Switching – Non-linearized Output

Figure 64 shows the output voltage and current of the converter, trying to operate a specified load rated for output power. The RMS voltage values presented in Figure 64 is of *116.4* V_{RMS} . Proportionally matching the design values, the RMS output current reached





As Figure 65 shows, the resultant voltage ripple of the output voltage in Figure 64 was of 48 V, matching the values for which the converter was designed.

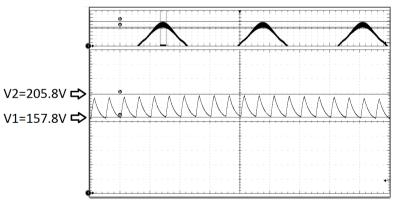


Figure 65 - Complementary SW - non-linearized voltage ripple. Source: Self-authorship

Figure 66 shows the output current ripple as 1.072 A.

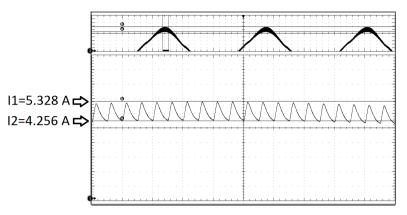


Figure 66 - Complementary SW - non-linearized current ripple. Source: Self-authorship

The acquisition shown in Figure 67 is the voltage across switch S_{1P} . The overvoltage in this waveform is product of the energy stored in the parasite inductances in both the primary and secondary windings of the flyback inductor. For this application, the clamping voltage was set to protect the switches without degrading the overall efficiency of the converter, which means that the clamp circuit was set approximately for voltages of *600 V*. Thus, the clamping voltage is not visible in the acquisition of the voltages on these switches.

Figure 68 shows the voltage in S_{2P} . The maximum voltage registered during this acquisition in S_{1P} was 376.5 V and 293.8 V in S_{2P} .

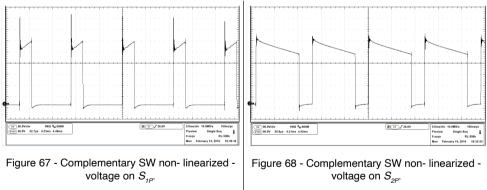






Figure 69 and Figure 70 present, respectively, the voltages on S_{1N} and S_{2N} . In this acquisition, the maximum voltage registered in S_{1N} was 363.2 V and in S_{2N} was 301.2 V.

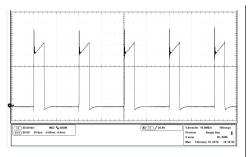
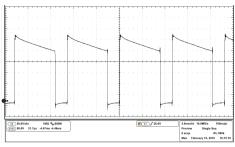
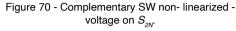


Figure 69 - Complementary SW non- linearized - voltage on $S_{\eta N}$

Source: Self-authorship

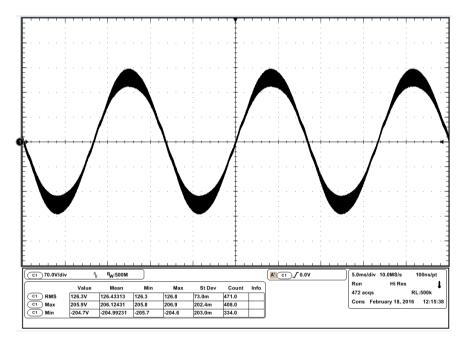




Source: Self-authorship

6.2 Complementary Switching – Linearized Output

According to section 3.4.1, a linearized output produces less harmonic content, ultimately leading to a lower THD. Therefore, the output voltage/current represents a better sinusoidal waveform. As Figure 71 shows, the converter reaches the desired 127 $V_{_{RMS}}$ output voltage.



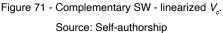
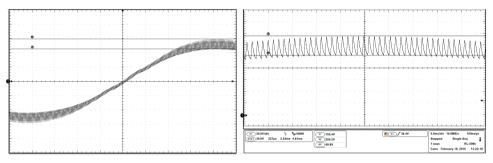
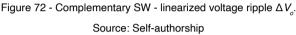


Figure 72 presents the voltage ripple zoomed in the crest of the sinusoidal waveform

of Figure 71. The markers in both images measure a maximum of 205.2 V and a minimum of 155.4 V, corresponding to a variation of $\Delta Vo=49.8$ V. This result shows good accuracy with the calculated and simulated values.





The acquisition presented in Figure 73 shows the output current of the converter and confirms the calculated value of the RMS current.

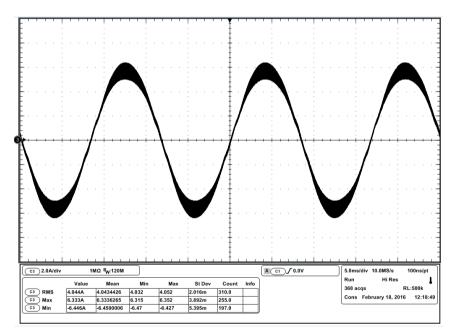


Figure 73 - Complementary SW - linearized I_o .

Source: Self-authorship

Figure 74 shows that both the output voltage and current obtained presents low harmonic distortion. The total harmonic distortion in the output voltage (*V-THD*) is 1.9%

and in the output current (*I-THD*) is 2 %, which is within the European norm IEC 61000-3-2 (Class A) and the North-American norm IEEE 519 (below 5%).

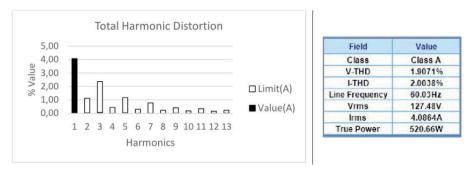
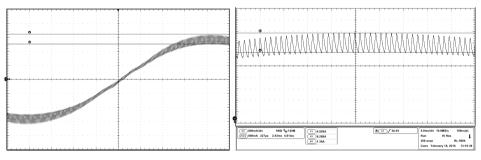


Figure 74 - Complementary switching strategy - total harmonic distortion. Source: Self-authorship

Figure 75 presents the waveform previously presented in Figure 73 zoomed in to show the current ripple. The distance between the markers measure a ripple of *1.4 A*, which coincides with the simulated and calculated values shown in Table 6.



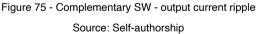


Figure 76 and Figure 77 show, respectively, the voltage on $S_{_{1P}}$ and $S_{_{2P'}}$. Both waveforms present the voltage on the switches when the output voltage is at its maximum, when a = $\frac{1}{2}$. The peak values in these acquisitions are 418.7 V in $S_{_{1P}}$ and 309.8 V in $S_{_{2P'}}$.

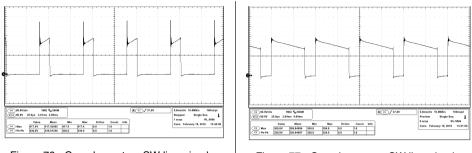


Figure 76 - Complementary SW linearized - voltage on $\mathcal{S}_{\mbox{\tiny 1P'}}$

Source: Self-authorship



Figure 78 shows the moment when S_{2P} turns off and S_{1P} turns on while the output voltage is maximum in a = $\pi/_{2P}$.

Similarly, Figure 79 shows when S_{1P} is blocked and S_{2P} turns on while the output voltage is maximum in a = n/2.

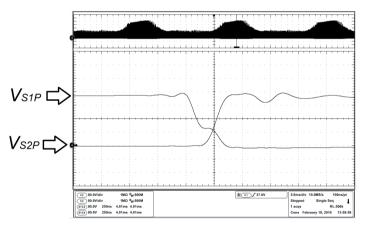


Figure 78 - Complementary SW linearized - $S_{_{2P}}$ off / $S_{_{1P}}$ on.

Source: Self-authorship

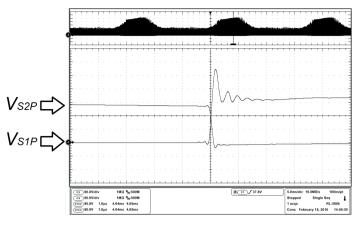


Figure 79 - Complementary SW linearized – $S_{_{1P}}$ off / $S_{_{2P}}$ on. Source: Self-authorship

The voltages on $S_{_{1N}}$ and $S_{_{2N}}$ are shown, respectively, in Figure 80 and Figure 81 for rated output power when the output voltage is at its negative peak. The maximum values in these acquisitions were 316.1 V on $S_{_{2N}}$ and 393.6 V on $S_{_{1N}}$.

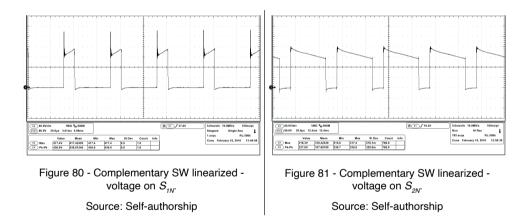


Figure 82 shows the moment when $S_{_{1N}}$ turns off and $S_{_{2N}}$ turns on. Similarly, Figure 83 shows the moment when $S_{_{2N}}$ turns off and $S_{_{1N}}$ turns on. Both acquisitions were performed when the output voltage were at its maximum in a = ${}^{3\pi}/{}_{_{2}}$.

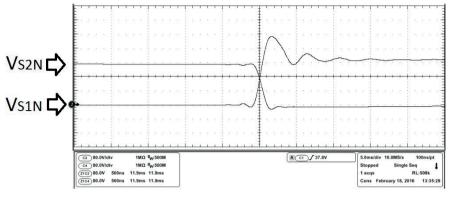


Figure 82 - Complementary SW linearized - $S_{_{1N}}$ off / $S_{_{2N}}$ on. Source: Self-authorship

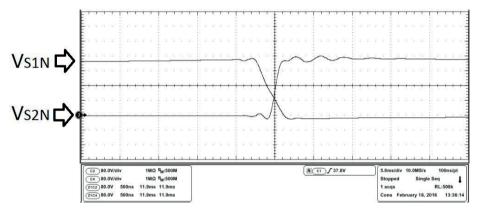
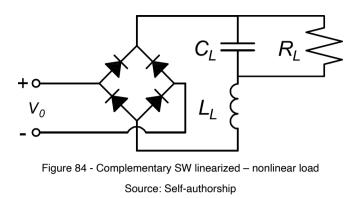


Figure 83 - Complementary SW linearized – S_{2N} off / S_{1N} on.

Source: Self-authorship

6.3 Complementary Switching Strategy – Nonlinear Load

As the experimentation progressed and the converter was performing well, a test with nonlinear load was carried out to test the converter's bidirectionality. The tested load is a single-phase full-wave bridge rectifier, circuit of Figure 84, and was composed of a 1 mH inductor as L_{L} and six electrolytic capacitors connected in parallel of 470 μ F / 400 V as CL. The resistance R_{L} is used to control the output power and limit the current.



The resultant output voltage and current are presented in Figure 85. The unbalance of the converter operating such output load is clear. Although the RMS voltage is 127 V, the maximum current is 6.56 A in the positive semi-cycle and -8.32 A in the negative semi-cycle. This characteristic, however, tends to be minimized once a controller is designed and the converter operates in closed-loop.

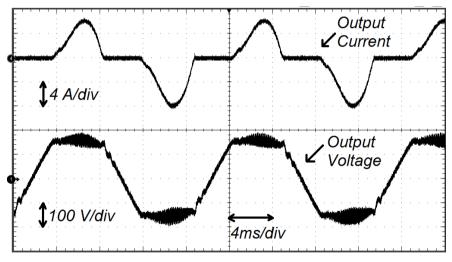


Figure 85 - Complementary SW linearized – nonlinear load output voltage and current. Source: Self-authorship

The unbalance and high voltage levels at the output of the converter, prevented the experiments to go further than 350 W, as the output voltage in these conditions were exceeding 190 V in the positive semi-cycle. In addition, the high harmonic distortion causes overheating in the components, particularly in the magnetics.

However, the voltages on the switches are proportional to the output power. Therefore, despite the distortion on the waveforms, the maximum values are similar. Figure 86 shows

the voltages on $S_{_{1P}}$ and $S_{_{2P}}$ zoomed-in the positive semi-cycle of the output voltage. The maximum values registered in this acquisition are 310 V on $S_{_{2P}}$ and 462 V on $S_{_{1P}}$. It is noticeable the difference in these values, however, if not by the voltage surge on $S_{_{1P}}$ when the switch blocks, the maximum values would be closer.

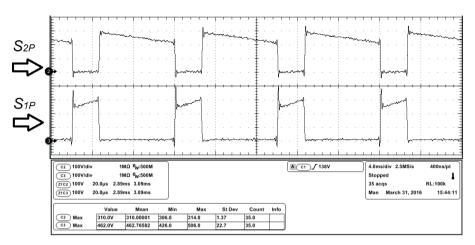


Figure 86 - Complementary SW nonlinear load - voltage on $S_{_{1P}}$ (100 V/div) and on $S_{_{2P}}$ (100 V/div). Source: Self-authorship

The same observations are true for the voltages on S_{1N} and S_{2N} presented in Figure 87. In this acquisition, the voltage on S_{1N} is 316 V and in S_{2N} is 452 V in the negative semicycle when the voltage is maximum.

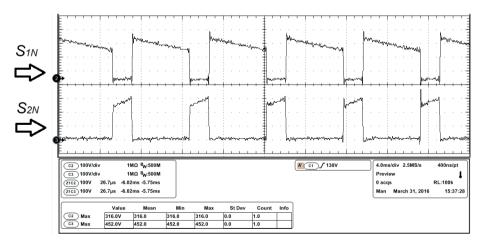


Figure 87 - Complementary SW nonlinear load - voltage on $S_{_{1N}}$ (100 V/div) and on $S_{_{2N}}$ (100 V/div). Source: Self-authorship

6.4 Alternative Switching Strategy – Non-linearized Output

Figure 88 shows the alternative switching operating a linear load with a non-linearized output. Similar to the non-linearized output voltage of the complementary switching strategy, the RMS output voltage only reached *97 VRMS*. The markers on Figure 89 shows a voltage ripple of 73 V (V1=143V / V2=216).

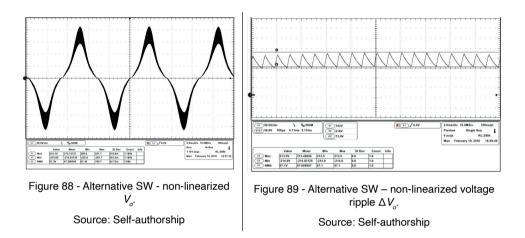


Figure 90 shows the non-linearized output voltage and current. Figure 91 presents the current waveform zoomed-in with a ripple of *1.926 A*.

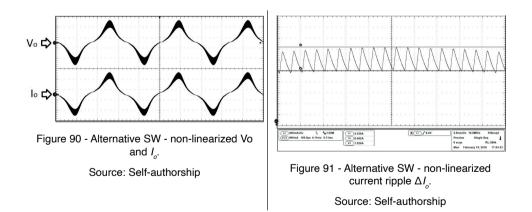


Figure 92 and Figure 93 shows the voltage over the switches $S_{_{1P}}$ and $S_{_{2P}}$ for a peak positive voltage output.

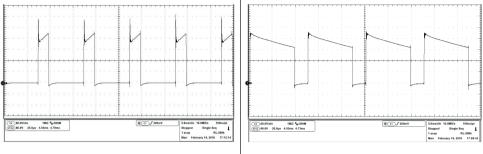


Figure 92 - Alternative SW non-linearized voltage over $\mathcal{S}_{\rm sp}$



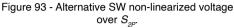




Figure 94 shows voltage on S_{1P} and S_{2P} in the transition of zero output voltage. Similarly, Figure 95 shows the voltage on S_{1N} and S_{2N} in the transition of zero output voltage.

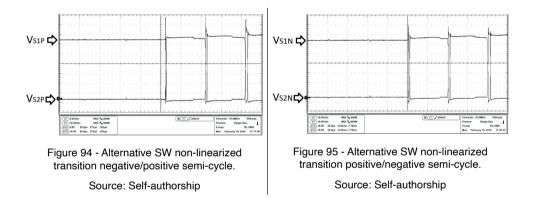
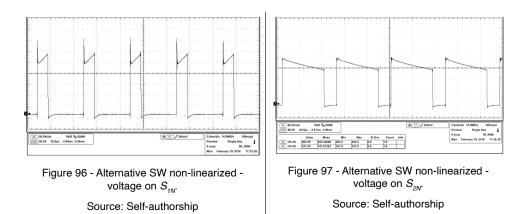
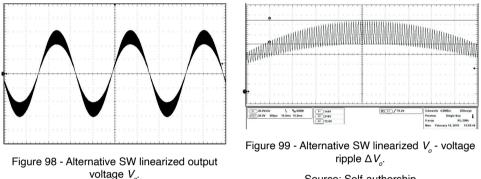


Figure 96 and Figure 97 show the voltages, respectively, on $S_{_{1N}}$ and $S_{_{2N^2}}$ when the output voltage is at its maximum in a = ${}^{_{3T}}/_{_{2N}}$, therefore in the negative semi-cycle.



6.5 Alternative Switching – Linearized Output

Once the output is linearized, the converter operates at its rated output power of *500 W* and both output voltage and current represents a sinusoidal waveform. Figure 98 shows the output voltage of the converter in $127 V_{RMS}$. The voltage ripple in Figure 99 is higher than the calculated because the prototype uses an equivalent output capacitance of $3 \mu F$, which should give a ripple of *67.35 V*. In this acquisition, the voltage ripple is *73 V*.



Source: Self-authorship



Figure 100 shows the output current of the converter operating a resistive load. In this acquisition, the output power of the converter was *528 W*, which explains why the RMS current in this figure is *4.149 A*. The calculated value for a similar output power returns *4.157 A*, which indicated good accuracy of calculations. Figure 101 presents the waveform from Figure 100 zoomed-in to show the ripple of the output current at *1.949 A*.

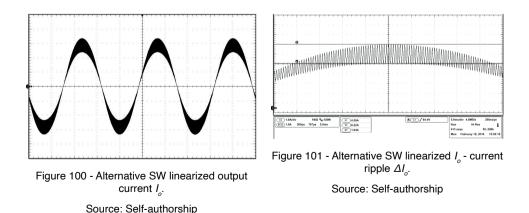
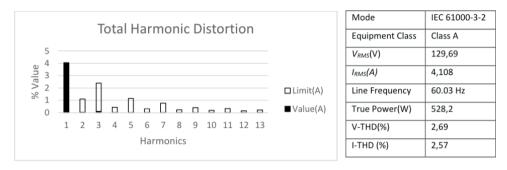
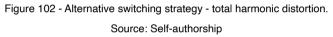


Figure 102 shows that both output voltage and current in the alternative switching strategy presents small harmonic distortion. However, even though this switching strategy

is still within both norms IEC 61000-3-2 (Class A) and IEEE 519 (below 5%), both values are higher than the results obtained for the complementary switching strategy, presented in Figure 74.





The waveform presented in Figure 103 and Figure 104 show the voltage measured, respectively, on $S_{_{1P}}$ and $S_{_{2P}}$ when the output voltage is at is maximum in a = $^{n}/_{_2}$. The peak voltage registered in this acquisition is 382.8 V for $S_{_{1P}}$ and 283.1 V in $S_{_{2P}}$. It is noteworthy that the peak voltage values of the alternative switching strategy are smaller in comparison to the complementary switching strategy, thus confirming the predictions made via calculation and simulation (see Table 8and Table 9).

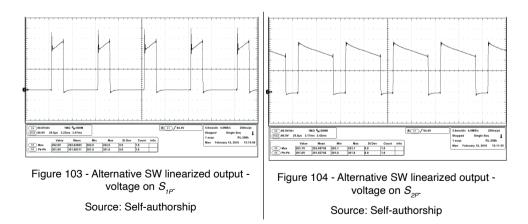


Figure 105 shows the juxtaposition of the voltage on S_{1P} and S_{2P} when S_{1P} turns off and S_{2P} turns on. This acquisition was made when the output voltage is at its maximum for a = "/₂, therefore, in the positive semi-cycle.

Similarly, Figure 106 shows the voltage on S_{2P} when it turns off and in S_{1P} when it turns on. This acquisition was made when the output voltage is at its maximum for a = $3\pi / 2$,

therefore, in the negative semi-cycle.

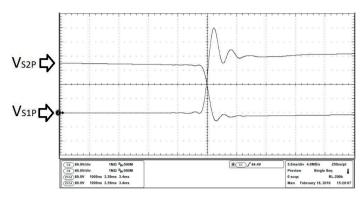
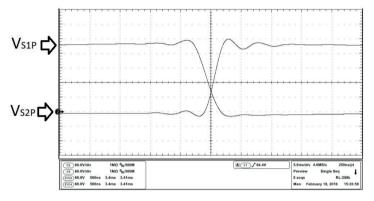


Figure 105 - Alternative SW linearized – S_{1P} off / S_{2P} on.

Source: Self-authorship



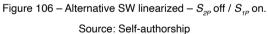


Figure 107 and Figure 108 show the voltage measurements on S_{1N} and S_{2N} , respectively, when the output voltage is at is maximum in a = $3\pi/_2$. The maximum voltage values registered in this acquisition on S_{1N} is 356.1 V and on S_{2N} is 289.9 V.

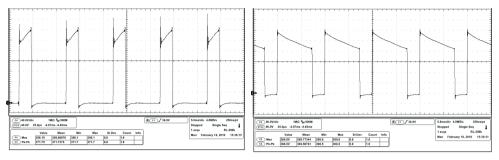
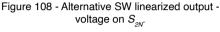
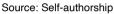


Figure 107 - Alternative SW linearized output - voltage on $S_{_{1N}}$.

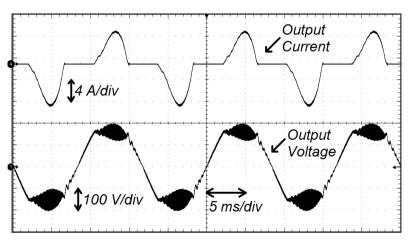
Source: Self-authorship

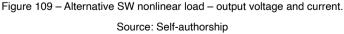




6.6 Alternative Switching Strategy – Nonlinear Load

The successful results presented thus far for the alternative switching strategy were considered satisfactory enough to assume that the bilinearity of the converter could be tested. Therefore, for the operation with nonlinear loads, the duty cycle of the converter had to be linearized, as the voltage spikes were too high when it was not. The resultant output voltage and current for a nonlinear load are presented in Figure 109.





Although in smaller scale, the unbalance of the current in this switching strategy is still present. In this case, the maximum current in Figure 109 is *6.169 A* and the minimum is *-7.853 A*.

6.7 Efficiency Tests

During the experiments, the efficiency of the converter was tested. The calculated curves in Figure 110 show that the approximations made to determine each component losses gave a close overview of what happens in the prototype. Further analysis on the losses generated by the RCD clamp circuit can be made to approximate the calculated curve with the actual experiment even more. All calculations made to obtain the curves are presented in Appendix C (complementary switching strategy) and Appendix E (alternative switching strategy) and were performed using only information available in the datasheet of the components.

As the experiments were performed, an efficiency curve was obtained for every tenth of the rated output power. These results are put into perspective with the calculated efficiency values, represented by the dashed lines, in Figure 110. In the complementary switching strategy, the values averaged a difference of 0.5 % from the calculated values to the experimental results in the range of 100 W to 500 W. In this case, all calculated values are higher than the experimental test results. The average difference in the alternative switching strategy is -0.5 % in the range of 50 W to 500 W. It is noteworthy that the curve described by the experimental results crosses the curve of calculated values in 450 W and, from this point onwards, tends to distance itself from the calculated curve. This is due to the oversizing of the conduction losses in the calculations. Thus, as the output power increases, the switching losses become more expressive, causing the crossing of the curves.

Overall, in the experimental test results, the alternative switching strategy presents an efficiency that varies from 2% to 2.6% higher than the complementary switching strategy. These results confirm the initial premise of the alternative switching strategy, showing that the reduction of the RMS current values and maximum voltages in all semiconductors are indeed a strong indicator of efficiency improvement.

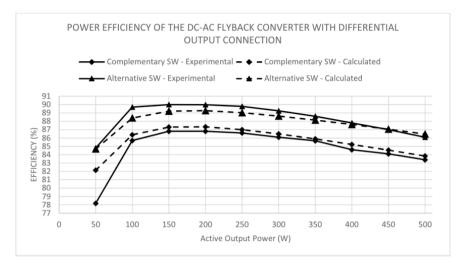


Figure 110 – Efficiency of the DC-AC flyback converter with differential output connection – linear load. Source: Self-authorship

Figure 111 compares the experimental test results obtained from both switching strategies for linear and nonlinear loads. Although the tests performed with nonlinear load for both switching strategies had to be aborted when the output power reached *350 W*, their respective curves show good fidelity to the curve obtained with linear loads.

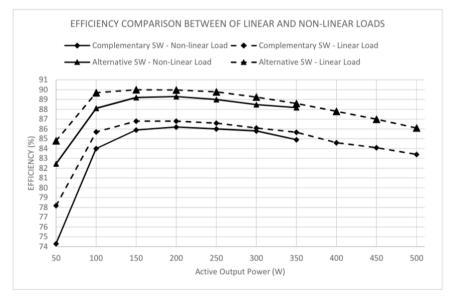


Figure 111 - DC-AC flyback converter with differential output connection – efficiency comparison between linear and nonlinear loads

Source: Self-authorship

7 | CONCLUSION

The converter presented in this chapter is an attractive alternative for a single- stage dc-ac converter. The open-loop results indicate that this converter is a well- suited off-line solution for simple applications that does not require closed-loop control as well as good potential for grid connection applications.

As expected, the alternative switching strategy increases the efficiency of the converter, presenting an average efficiency of *86.4* % in rated output power. It is noteworthy, that it would be necessary two converters with *93* % of efficiency to process the same output power in a two-stage configuration. It was verified that the superiority of the efficiency levels were achieved not only because of the reduced RMS currents in all semiconductors, but also by the significant reduction of the voltage spikes, particularly on S_{1p} and S_{1pr} .

On the other hand, the same prototype operating the complementary switching strategy presents an average efficiency of 83.4 % for rated output power. Although the results are not as satisfactory, once put into the perspective of a two-stage configuration, it would require two converters operating with an average power efficiency of 91.3 % to produce the same overall result.

A setback of this topology, regardless of the switching strategy used, is that the hard switching causes a considerable voltage surge in both switches on the primary windings of the flyback inductors. In a bid to improve the efficiency, the converter was tested using the MOSFET SPW47N60C3 and better results were achieved, peaking an efficiency of *88.1* % for rated output power for the alternative switching strategy. However, issues with the driver technology used did not allow the converter to operate smoothly, causing shut down events as the magnetics heat up. It is important to call attention to the potential of the converter if better switches and driver technologies are implemented or if the turns ratio of the flyback inductor is used in favor of one or another switching strategy. It is still worth mentioning that, during the tests performed with nonlinear loads, the observed unbalanced output needs to be investigated as to whether it is an intrinsic characteristic of the prototype built, which can be minimized with a controller in closed-loop operation, or if it is intrinsic to the topology/switching strategies tested. Part of this behavior can be observed with linear loads; however, this problem was emphasized with nonlinear loads.

At this point, some new considerations had to be made towards the sequence of this research. On the one hand, original contributions, such as the alternative switching strategy and the transfer functions of the converter coupled to an output voltage source for both switching strategies were performed and validated by means of simulation. On the other hand, the efficiency levels demonstrated by the converter were not considered overwhelmingly satisfactory, to the point of investing a considerable amount of time to perform the connection of the converter to the utility grid.

Consequently, the direction adopted for the progress of this research was towards

a new single-stage topology capable of solving the problem caused by the voltage surge in the primary windings of the flyback inductors, as an attempt to increase the power efficiency levels. The purpose of this new converter is to study a new topology with potential of being integrated to the utility grid and operating in higher switching frequencies by means of softswitching techniques. Chapter 4 presents the static analysis, currents and voltages in all components and control to output transfer function.

ACTIVE-CLAMPING SINGLE-STAGE FLYBACK CONVERTER

The flyback converter is a topology that offers simplicity of design and ease of control while keeping a low component count. In Chapters 2 and 3, the dc-ac flyback converter presented confirms the simplicity of design that the topology can offer as an alternative for grid-tied converters. However, because of the voltage spikes caused by the leakage inductance and hard switching of the main switch, which often leads to reduced efficiency levels; usually, the converter is restricted to applications of low output power. This phenomenon is shown in Figure 67 and Figure 69 for the complementary switching strategy and in Figure 103 and Figure 107 for the alternative switching strategy. As an alternative to solve this problem, many authors have researched different ways to clamp the voltage spike at the main switch, while others invest in soft-switching techniques. This chapter presents an active-clamping circuit to reduce the voltage spikes, offering zero voltage switching (ZVS) for the main switch.

1 | INTRODUCTION

From all possible uses of a flyback converter as a single-stage dc-ac converter, simply known as flyback inverter, one particular inverter base topology has attracted special attention from the research community¹.

For renewable energy applications, mainly for solar energy applications, simple bidirectional approaches have been explored, as presented in (SUKESH, PAHLEVANINEZHAD e PRAVEEN, 2013), (SARANYA e CHANDRAN, 2015) and in Figure 112. In these cases, similar to the flyback converter presented in Chapter 3, the leakage inductance is a problem that can cause overvoltage across the switches as the main transistor turns off, potentially causing the destruction of the switch or, in contrast, oversizing the switch to bear the overvoltage.

RCD clamps can address this problem offering a direct and simple solution, although resulting in reduced levels of efficiency. In this case the energy stored in the leakage inductance ends up dissipated as heat, resulting in significant power loss, as affirmed by (IIDA e BHAT, 2005) and exemplified by the prototype built for the experimental results presented in Chapter 3.

^{1 (}KASA, IIDA e CHEN, 2005), (MUKHERJEE, PAHLEVANINEZHAD e MOSCHOPOULOS, 2014), (ABRAMOVITZ, CHIH-SEHNG e SMEDLEY, 2013), (ABRAMOVITZ, HEYDARI, *et al.*, 2014), (SARANYA e CHANDRAN, 2015), (MO, CHEN, *et al.*, 2011), (KIM, KIM, *et al.*, 2011), (JOHNY e SHAFEEQUE, 2014), (IIDA e BHAT, 2005), (SHIMIZU, WADA e NAKAMURA, 2006)

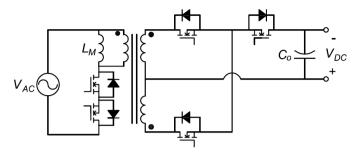


Figure 112 - Bidirectional flyback inverter. Source: Self-authorship

In (IIDA e BHAT, 2005) and Figure 113, a flyback inverter that reduces the leakage inductance effect in the main switch is proposed. The technique, called switched snubber circuit or primary current steering, makes use of the leakage inductance of the flyback inductor to achieve zero voltage transition in the main switch. The prototype build in this case operates with a *30 V* of input voltage, *100 V* of output voltage, switched at *50 kHz* and output power of *100 W*. While connected to the utility grid, the efficiency with *70 W* of output power is approximately *84* %.

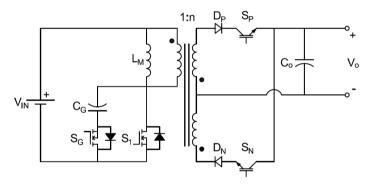


Figure 113 - Flyback inverter with LC snubber. Source: Self-authorship

In order to improve the efficiency of the topology even further, in (ABRAMOVITZ, CHIH-SEHNG e SMEDLEY, 2013), (VARTAK, ABRAMOVITZ e SMEDLEY, 2014) and (MUKHERJEE, PAHLEVANINEZHAD e MOSCHOPOULOS, 2014) a regenerative snubber circuit is proposed. By adding an auxiliary winding to the flyback inductor, the leakage inductance can be used to achieve soft switching. The main advantage of this technique is that it does not need an additional discrete inductor, sparing area in the PCB while achieving better performance levels. In (MUKHERJEE, PAHLEVANINEZHAD e MOSCHOPOULOS, 2014), a prototype is presented with an input voltage of 45 VDC, output voltage of 110 V_{RMS}

and restricted to a maximum output power of *100 W*. The specific switching frequency as well as the efficiency levels registered were not reported. Figure 114 shows the topology of the inverter studied by (MUKHERJEE, PAHLEVANINEZHAD e MOSCHOPOULOS, 2014).

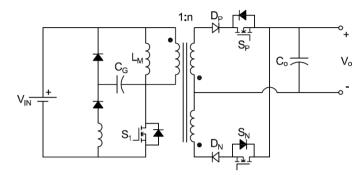
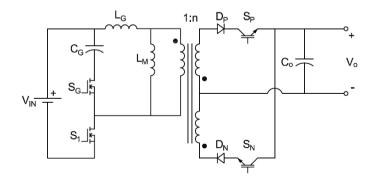
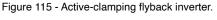


Figure 114 - Flyback inverter with regenerative snubber. Source: Self-authorship

In this chapter, an active-clamping circuit for the flyback inverter operating in continuous conduction mode (CCM) is presented. The inverter makes use of an additional discrete inductor in the primary winding to achieve ZVS on both switches of the circuit. Theoretically, the switches in the circuit of the secondary windings can also achieve ZVS during the zero voltage transition of the ac output. The switching strategy adopted is a high frequency complementary switching between the main and the auxiliary switches (*S1* and *SG*), and grid frequency for the switches in the secondary windings of the converter. The circuit of the proposed inverter is presented in Figure 115. It is worth noting that this topology is not bidirectional as the previous structure presented in Chapters 2 and 3 were. This is due to a design choice of operating with only four switches, considering that a bidirectional topology would require the diodes *DP* and *DN* to be replaced for switches.





Source: Self-authorship

21 SWITCHING STRATEGY

Figure 115 presents the main circuit configuration of the single-stage active- clamping dc-ac flyback converter. The circuit consists of two switches in the primary winding, being *S1* the main switch and S_G the auxiliary; a flyback inductor with its magnetizing inductance L_M and turns ratio of 1:*n*; a discrete auxiliary switching inductor L_G ; and an auxiliary capacitor for active-clamping C_G . In the secondary windings, there are two blocking diodes D_ρ and D_N ; two control switches S_ρ and S_N ; and a capacitor C_Q acting as output filter.

Switches S_{r} and S_{G} are switched complementarily, so that the converter operates in CCM. Switches S_{P} and S_{N} provide the path to the output ac current, in order to generate positive and negative semi-cycles, respectively. Figure 116 presents one switching cycle of the switching strategy adopted for this converter. In Figure 116 (A), the output voltage of the converter is in the positive semi-cycle due to the command in S_{P} . The semi-cycle of the converter changes to negative when S_{P} is turned off and S_{N} is turned on, as in Figure 116 (B).

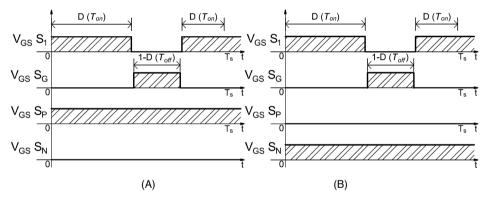


Figure 116 - Active clamp flyback inverter - switching strategy (A) for $V_{\sigma}>0$ (B) for $V_{\sigma}>0$. Source: Self-authorship

3 | OPERATING STAGES

To simplify the analysis of the inverter, all semiconductors are considered ideal, the flyback inductor is modeled as an ideal transformer with its magnetizing inductance represented by L_{M} and turns ratio of *1:n*. Both secondary windings of the inductor have the same number of turns.

In the first operating stage (see Figure 117), switch S_{γ} is turned on. Therefore, the input voltage V_{IN} charges the magnetizing and clamp inductances, respectively L_{M} and L_{G} , as the current circulates through S_{γ} . Diode D_{P} blocks the output voltage V_{O} , while the output capacitor *Co* discharges itself to the output load.

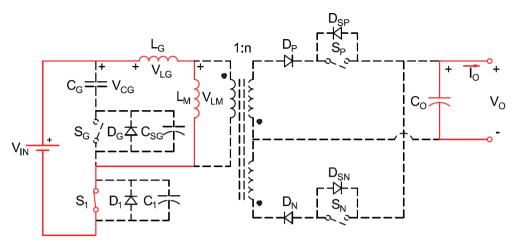


Figure 117 - Active-clamping flyback converter - first operating stage V_{o} >0. Source: Self-authorship

The second operating stage begins when *S1* is turned off. The current in *LG* finds its way through C_{1} and C_{SG} , charging and discharging them, respectively. This stage ends as soon as the voltage across *SG* reaches zero. Figure 118 shows the equivalent circuit for the second operating stage.

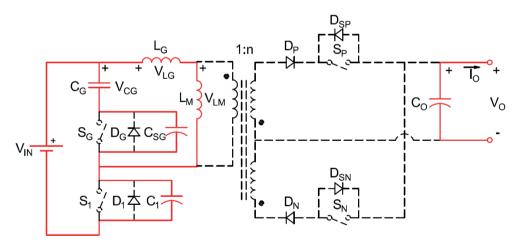


Figure 118 - Active-clamping flyback converter – second operating stage V_{σ} >0. Source: Self-authorship

The third stage (Figure 119) starts when D_G becomes forward biased. In such condition, the current through L_G is directed to the clamping capacitor C_G , thus enabling the circuit to recover the energy stored in this element. It is noteworthy that S_G must be turned on during this stage to guarantee ZVS condition for this component. This stage lasts until

the current through L_{G} reaches zero.

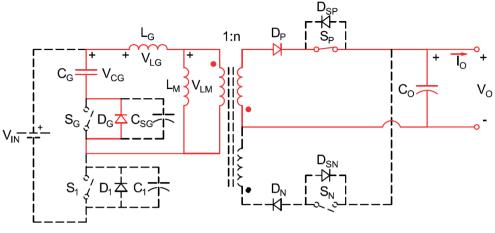
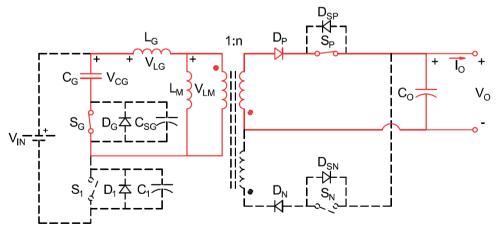
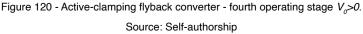


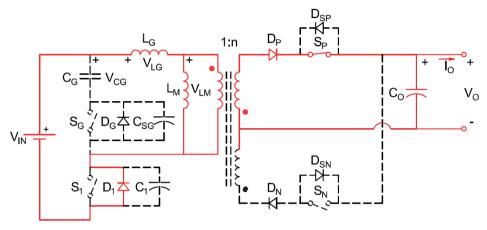
Figure 119 - Active-clamping flyback converter - third operating stage V_{σ} >0. Source: Self-authorship

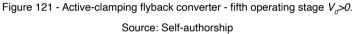
Considering that the current in L_{g} tends to zero during the third operating stage, S_{g} has to turn on to start the fourth operating stage before the current becomes null, allowing it to assume negative values. During the fourth operating stage, S_{p} and D_{p} are still turned on, discharging the current of the magnetizing inductance in the secondary winding and to the output load. Figure 120 presents the equivalent circuit of the converter during this operating stage.





The withdrawal of the command pulse from *SG* starts the fifth operating stage (see Figure 121). In order to preserve its continuous behavior, the current in L_{G} starts flowing through C_{I} and C_{SG} , discharging and charging them, respectively. When the voltage across S_{I} becomes null, this stage is finished.





At the beginning of the sixth stage (Figure 122), *D1* becomes forward biased. When this operating stage begins, the current in L_G is at its minimum value on the up turn to zero and positive values, offering ZVS condition to S_1 as the current circulates through C_1 . Therefore, as soon as the current though L_G becomes null, this stage ends.

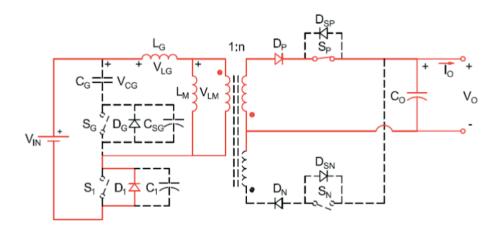


Figure 122 - Active-clamping flyback converter - sixth operating stage V_{o} >0. Source: Self-authorship

As the current in L_g reaches zero, the seventh operating stage begins (Figure 123). Since the value of the current in L_g is lower than the current in L_M , D_P remains forward biased. When these currents become equivalent, D_P blocks and finishes this stage.

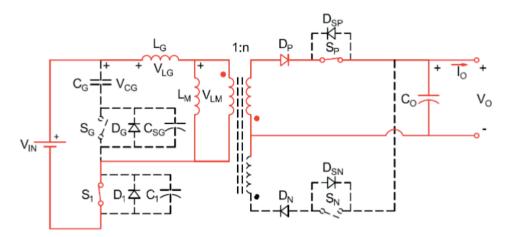


Figure 123 - Active-clamping flyback converter - seventh operating stage V_{o} >0. Source: Self-authorship

4 | STATIC ANALYSIS

Figure 124 presents typical waveforms within a switching cycle for both the active clamp inductor and magnetizing inductance currents and voltages, respectively, I_{LG} , V_{LG} , I_{LM} and V_{LM} as well as the current I_{DP} in the blocking diode D_{P} . The waveforms presented consider the converter's operation as an output voltage step-up operating in continuous conduction mode. The values presented in these waveforms are obtained from the mesh analysis of the equivalent circuit for each operating stage, which are important to determine the duration of the operating stages.

To simplify the analysis of the converter, the second and fifth operating stages are taken out of the analysis due to its low contribution in terms of voltage and current variations and for its short duration. The sum of the operating stages where S_{τ} is turned on corresponds to the total time in which DT_s has been attributed, in this case the first, sixth and seventh operating stages, as given by (4.1).

$$\Delta t_1 + \Delta t_6 + \Delta t_7 = DT_s \tag{4.1}$$

For *Ts* is the switching period, established by the switching frequency f_s . The remaining operating stages in one switching cycle corresponds to $(1-D)T_s$, thus resulting in (4.2).

$$\Delta t_3 + \Delta t_4 = (1 - D)T_s \tag{4.2}$$

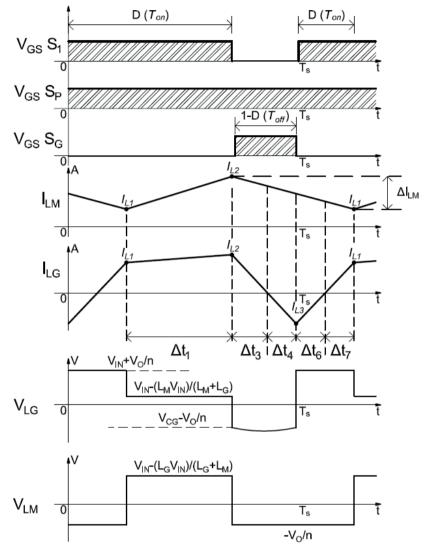


Figure 124 - Typical operating waveforms for the positive semi-cycle. Source: Self-authorship

Due to the variation of the current in the magnetizing inductance in one switching period, it is crucial to define the length of each operating stage so the converter can operate within certain requirements.

The voltage on the auxiliary inductance L_{g} , presented in Figure 124 and transcript to (4.3), can define the duration of the first operating stage.

$$V_{LG} = V_{IN} - V_{LM}$$
(4.3)

Where *VIN* is the input voltage, V_{LM} and V_{LG} are the voltages on the magnetizing (*LM*) and auxiliary inductances (L_G), respectively, during the first operating stage. Considering that $V_L = L^{di}L'_{dt}$, the time variation of the first operating stage, based on the current in the auxiliary inductance, presented in (4.3), is defined as given by (4.4).

$$\Delta t_1 = \frac{L_G \left(I_{L2} - I_{L1} \right)}{V_{IN} - V_{LM} \left(\Delta t_1 \right)}$$
(4.4)

In (4.4), I_{L1} and I_{L2} are the two currents identified in Figure 124 for I_{LM} and I_{LG} in the first operating stage.

Neglecting the time variation of the second operating stage makes the duration of Δt_3 and Δt_4 equal, because the voltage over the auxiliary and magnetizing inductance are equal during both operating stages. Considering that the sum of both third and fourth operating stages results in the total time in which S_7 is turned off, the time length of each operating stage corresponds to half the time where *SG* is turned on. Therefore, Δt_3 and Δt_4 are defined as given by (4.5).

$$\Delta t_3 = \Delta t_4 = \frac{(1-D)}{2f_s} \tag{4.5}$$

The duration of the seventh operating stage is taken from the variation of the current in the magnetizing inductance presented in Figure 124 and transcript to (4.6).

$$V_{LG}(\Delta t_{7}) = V_{IN} + \frac{V_{0}}{n}$$
(4.6)

From (4.6), the relationship $V_L = L^{di_L}/_{dt}$ defines the time variation of the seventh operating stage as given by (4.7).

$$\Delta t_7 = \frac{L_G I_{L1}}{V_{IN} + \frac{V_0}{n}}$$
(4.7)

The duration of the sixth operating stage, is obtained by substituting equations (4.4) and (4.7) in (4.1). This operation results in (4.8).

$$\Delta t_{6} = \frac{V_{IN}D + D^{V_{0}}/n - V_{0}/n}{2f_{s}\left(V_{IN} + V_{0}/n\right)}$$
(4.8)

Once the duration of each operating stage is known, important variables that define the operation of the converter must be defined, such as the current variations on

the magnetizing inductance, used to determine the duration of the operating stages. The analysis of the circuit during the first operating stage indicates that the current flowing through the magnetizing inductance is the same current that flows through the auxiliary inductance (see Figure 117). Equation (4.9) shows the relation of this current in the first operating stage.

$$I_{LG} = I_{LM} \tag{4.9}$$

Concerning the voltages during the first operating stage, (4.10) shows the relationship of the voltages across $L_{_{M}}$ $L_{_{G}}$ and the input voltage.

$$V_{LG} + V_{LM} = V_{IN}$$
(4.10)

As a function of voltages and inductances, equation (4.9) can also be written as given by (4.11).

$$\frac{V_{LG}}{L_G} = \frac{V_{LM}}{L_M} \tag{4.11}$$

Using (4.10) in (4.11) the voltages VLG and VLM are, respectively, defined in (4.12) and (4.13).

$$V_{LG} = \frac{L_G V_{IN}}{L_G + L_M}$$
(4.12)

$$V_{LM} = \frac{L_M V_{IN}}{L_G + L_M}$$
(4.13)

Once the equations that determine the voltage values in the magnetizing and auxiliary inductances during the first operating stage are known, the currents I_{L1} and I_{L2} from Figure 124 are obtained from the inductor's voltage equation. Therefore, considering that $V_{LG}/L_{G} = (I_{L2} - I_{L1})/\Delta t_{1}$, another expression that defines Δt_{1} is obtained as given by (4.14).

$$\Delta t_1 = \frac{(I_{L2} - I_{L1})(L_G + L_M)}{V_{IN}}$$
(4.14)

The current $I_{L2^{n}}$ presented in (4.15) is obtained by substituting (4.7), (4.8) and (4.14) in (4.1).

$$I_{L2} = \frac{\left(\frac{D}{f_s} - \frac{L_G I_{L1}}{V_{IN} + \frac{V_0}{n}}\right) V_{IN} \left(V_{IN} + \frac{V_0}{n}\right) + \left(L_G + L_M\right) \left(V_{IN} + \frac{V_0}{n}\right) I_{L1}}{V_{IN} L_G + \left(L_G + L_M\right) \left(V_{IN} + \frac{V_0}{n}\right)}$$
(4.15)

The unknown variable I_{L1} from equation (4.15) is obtained from the principles of the

Volt-second balance in $L_{\mu\nu}$ which reads as in (4.16).

$$\Delta t_1 \left(V_{IN} - V_{LG} \right) + \Delta t_3 \left(\frac{-V_0}{n} \right) + \Delta t_4 \left(\frac{-V_0}{n} \right) + \Delta t_6 \left(\frac{-V_0}{n} \right) + \Delta t_7 \left(\frac{-V_0}{n} \right) = 0 \quad (4.16)$$

From this point onwards, in order to simplify the equations presented, the inductance factor in (4.17) is used.

$$\lambda = \frac{L_G}{L_M} \tag{4.17}$$

The variable I_{L1} is then obtained from (4.16) by performing the substitution of Δ_{t1} as presented in (4.14), Δt_3 and Δt_4 as in (4.5), Δt_6 as in (4.7), Δt_7 as in (4.7), I_{L2} as in (4.15) and finally V_{LG} as in (4.12). It is noteworthy that V_{LG} in (4.16) refers to the average voltage over L_G only during the first operating stage. The current I_{L1} is defined as given by (4.18)

$$I_{L1} = \frac{\lambda \left(V_{IN} \left(D - 2 \right)^{V_0} / n + \frac{V_0}{n} / (D - 1) \right) + D \left(V_{IN} + \frac{V_0}{n} \right)^2 - \frac{V_0}{n} \left(V_{IN} + \frac{V_0}{n} \right)}{2\lambda f_s \left(L_G \frac{V_0}{n} + L_M \left(V_{IN} + \frac{V_0}{n} \right) \right)}$$
(4.18)

Once the variable I_{L1} is known, the current I_{L2} defined in (4.15) can be re-written as presented in (4.19).

$$I_{L2} = \frac{DV_{IN} + D\frac{V_0}{n} - \frac{V_0}{n}}{2L_G f_s}$$
(4.19)

The current in the auxiliary inductance, In Figure 124, varies from I_{L1} to I_{L2} during the first operating stage and from I_{L2} to I_{L3} in the third and fourth operating stages. Because of the absence of the second and fifth operating stages in the equations, the current I_{L3} is considered the negative value of I_{L2} , as (4.20) defines.

$$I_{L3} = -I_{L2} (4.20)$$

Because the converter operates in continuous conduction mode, the average current in the magnetizing inductance is the arithmetic average of I_{L1} and I_{L2} . Thus, the variation of the current in the magnetizing inductance is described as the difference between the maximum and minimum points of the variation, namely I_{L2} and I_{L1} , respectively, divided by the average current in the magnetizing inductance, as given by (4.21).

$$\Delta I_{LM} = \frac{2(I_{L2} - I_{L1})}{I_{L1} + I_{L2}}$$
(4.21)

The simplified equation that defines the variation of the current in the magnetizing inductance in terms of the inductance factor and static gain (M) is presented in (4.22).

$$\Delta I_{LM} = \frac{2\lambda M}{(M+1)(D-M+DM-\lambda M+D\lambda M)}$$
(4.22)

From the analysis of the converter, one can allege that the average output current of the converter is the same as the average current in the diode D_{P} in the positive semi-cycle. However, according to the waveform presented in Figure 124, it is necessary to know the variable I_{Lx} to obtain the equation that defines the average current in D_{P} . On the other hand, I_{Lx} is component of the linear transition from I_{L2} to I_{L1} , given by (4.23).

$$I_{Lx} = \frac{I_{L1}(\Delta t_3 + \Delta t_4) + I_{L2}(\Delta t_6 + \Delta t_7)}{\Delta t_3 + \Delta t_4 + \Delta t_6 + \Delta t_7}$$
(4.23)

The average output current (I_{ρ}) is written as the average current in D_{ρ} , as in (4.24).

$$I_0 = \frac{I_{L2} + I_{Lx}}{n}$$
(4.24)

By substituting (4.19), (4.23) and its respective time variations ($\Delta t_3, ..., \Delta t_7$) in (4.24), the output current is given by (4.25).

$$I_{0} = \frac{\left(V_{IN}L_{M}D + L_{G}D^{V_{0}}/_{n} + L_{M}D^{V_{0}}/_{n} - L_{G}^{V_{0}}/_{n} - L_{M}^{V_{0}}/_{n}\right)V_{IN}}{\left(V_{IN}L_{M} + L_{G}^{V_{0}}/_{n} + L_{M}^{V_{0}}/_{n}\right)2L_{G}f_{s}}$$
(4.25)

The equation of the output current, presented in (4.25), per-unit is defined in (4.26) and given by (4.27).

$$\overline{I_0} = \frac{2f_s L_G n I_0}{V_{IN}}$$
(4.26)

$$\overline{I_0} = \frac{D + D\lambda M + DM - M(\lambda + 1)}{1 + M\lambda + M}$$
(4.27)

Another unknown variable presented in Figure 124 is the voltage V_{CG} , which corresponds to the voltage on the auxiliary capacitor C_{G} . This variable is present in the voltage analysis of the magnetizing inductance (V_{LM}) in the third and fourth operating stages. Therefore, the duration of the third operating stage can be defined by the voltage variation on the magnetizing inductance as given by (4.28).

$$\Delta t_3 = \frac{-L_G I_2}{V_{CG} + \frac{V_0}{n}}$$
(4.28)

Considering that the third and fourth operating stages have the same duration, by

substituting equation (4.28) in (4.2), V_{CG} is obtained as presented in (4.29).

$$V_{CG} = \frac{-2f_s L_G \left(\left(\frac{D}{f_s} - \frac{L_G I_{L1}}{b} \right) V_{IN} \left(V_{IN} + \frac{V_0}{n} \right) + \left(L_G + L_M \right) \left(V_{IN} + \frac{V_0}{n} \right) I_{L1} \right)}{(1 - D) \left(V_{IN} L_G + \left(L_G + L_M \right) \left(V_{IN} + \frac{V_0}{n} \right) \right)} - \frac{V_0}{n}$$
(4.29)

The voltage on the auxiliary switching capacitor (V_{CG}) in (4.29) is simplified by substituting the current $I_{I,T}$, from (4.18), which gives (4.30).

$$V_{CG} = \frac{-DV_{IN}}{1-D}$$
(4.30)

Finally, of all the equations presented there are two unknown variables remaining, namely, the inductance factor (λ) and the operating duty cycle (D). These two variables are obtained from the evaluation of the minimum value that satisfies equations (4.22) and (4.27), considering that the voltage conversion ratio, the current ripple in the magnetizing inductance and the auxiliary switching inductor are initial design requirements.

However, once the converter operates an AC output, the static gain varies with the same angle of the sinusoidal output voltage. Therefore, the duty cycle needs to follow this angular variation in order to produce the desired AC output. The voltage conversion ratio adopted is presented by (4.31).

$$q(\alpha) = M\sin(\alpha) \tag{4.31}$$

The equation of the duty cycle is then obtained by isolating *D* from (4.27) and substituting *M* for *q* (a), as given by (4.31), in order to obtain the desired alternate output. The duty cycle of the switches located in the primary winding of the flyback inductor, namely S_{1} and S_{G} , is defined in (4.32).

$$D(\alpha) = \frac{\left| \overline{I_0}(\alpha) \left[q(\alpha)\lambda + q(\alpha) + 1 \right] + q(\alpha) \left[\lambda + 1 \right]}{q(\alpha)\lambda + q(\alpha) + 1} \rightarrow 0 < \alpha < \pi \right.}{\left. -\overline{I_0}(\alpha) \left[-q(\alpha)\lambda - q(\alpha) + 1 \right] - q(\alpha) \left[\lambda + 1 \right]}{-q(\alpha)\lambda - q(\alpha) + 1} \rightarrow \pi < \alpha < 2\pi \right.}$$
(4.32)

However, *DP* and *SP* are switched only when a varies from 0 to π , whilst D_N and S_N are switched only when α varies from π to 2π , as given by (4.34) for the former and by (4.33) for the latter.

$$D_{P}(\alpha) = \frac{\overline{I_{0}}(\alpha) \left[q(\alpha)\lambda + q(\alpha) + 1\right] + q(\alpha) [\lambda + 1]}{q(\alpha)\lambda + q(\alpha) + 1} \to 0 < \alpha < \pi$$

$$(4.33)$$

$$D_{N}(\alpha) = \begin{vmatrix} 0 \to 0 < \alpha < \pi \\ -\overline{I_{0}}(\alpha) \left[-q(\alpha)\lambda - q(\alpha) + 1 \right] - q(\alpha) \left[\lambda + 1\right] \\ -q(\alpha)\lambda - q(\alpha) + 1 \end{vmatrix} \to \pi < \alpha < 2\pi$$
(4.34)

5 | AUXILIARY SWITCHING INDUCTOR (LG)

The duration of each one of the operating stages varies along the variation of a in order to produce the desired alternate output. Therefore, the currents identified as I_{L1} and I_{L2} , defined by equations (4.18) and (4.19), respectively, presents different values as a varies from zero to 2π . Considering this, I_{L1} is rewritten as presented in (4.35).

$$I_{L1}(\alpha) = \frac{\lambda \left(V_{IN} \frac{V_0(\alpha)}{n} D(\alpha) + \left(\frac{V_0(\alpha)}{n} \right)^2 (D(\alpha) - 1) \right) + D(\alpha) \left(V_{IN} + \frac{V_0(\alpha)}{n} \right) - \frac{V_0(\alpha)}{n} \left(V_{IN} + \frac{V_0(\alpha)}{n} \right)}{n} \rightarrow 0 < \alpha < \pi}$$

$$I_{L1}(\alpha) = \frac{\lambda \left(V_{IN} \frac{-V_0(\alpha)}{n} D(\alpha) + \left(\frac{-V_0(\alpha)}{n} \right)^2 (D(\alpha) - 1) \right) + D(\alpha) \left(V_{IN} - \frac{V_0(\alpha)}{n} \right) + \frac{V_0(\alpha)}{n} \left(V_{IN} - \frac{V_0(\alpha)}{n} \right)}{2\lambda f_s \left(\frac{-V_0(\alpha)}{n} L_G + L_M \left(V_{IN} - \frac{V_0(\alpha)}{n} \right) \right)} \rightarrow \pi < \alpha < 2\pi$$

$$(4.35)$$

It is noteworthy that both equations presented in (4.35) are essentially the same as in (4.18), although because of the polarity dot of the flyback inductor, the output voltage changes its signal for $V_o < 0$ when $\pi < \alpha < 2\pi$. The same consideration applies to the current I_{L2} presented initially in (4.19). Considering this, (4.36) presents an equation for I_{L2} that assumes the variations of a from zero to 2π .

$$I_{L2}(\alpha) = \frac{V_{IN}D(\alpha) + D(\alpha)\frac{V_0(\alpha)}{n} - \frac{V_0(\alpha)}{n}}{2L_G f_s} \to 0 < \alpha < \pi$$

$$\frac{V_{IN}D(\alpha) + D(\alpha)\frac{-V_0(\alpha)}{n} + \frac{V_0(\alpha)}{n}}{2L_G f_s} \to \pi < \alpha < 2\pi$$
(4.36)

Once these current values as known, the duration of each operating stage can be rewritten to assume its duration for any given angle alpha. Initially defined in (4.14) the duration of the first operating stage is given by (4.37).

$$\Delta t_1(\alpha) = \frac{(I_{L2}(\alpha) + I_{L1}(\alpha))(L_G + L_M)}{V_{IN}}$$
(4.37)

Similarly, Δt_3 (α) and Δt_4 (α) are written as the duty cycle changes its values for any given angle alpha, as presented in (4.38).

$$\Delta t_3(\alpha) = \Delta t_4(\alpha) = \frac{1 - D(\alpha)}{2f_s}$$
(4.38)

Considering that the duration of the operating stages are obtained by the analysis of the current in the auxiliary switching inductor, it is worth noticing that the considerations made in regard to the voltage variation in the secondary winding for currents I_{L1} (α) and I_{L2} (α) are valid for all operating stages as well. Therefore, the duration of the sixth operating stage is given by (4.39).

$$\Delta t_{6}(\alpha) = \frac{\left| \frac{V_{IN}D(\alpha) + D(\alpha)\frac{V_{0}(\alpha)}{n} - \frac{V_{0}(\alpha)}{n}}{2f_{s}\left(V_{IN} + \frac{V_{0}(\alpha)}{n}\right)} \rightarrow 0 < \alpha < \pi \right.}{\left| \frac{V_{IN}D(\alpha) + D(\alpha)\frac{-V_{0}(\alpha)}{n} + \frac{V_{0}(\alpha)}{n}}{2f_{s}\left(V_{IN} - \frac{V_{0}(\alpha)}{n}\right)} \rightarrow \pi < \alpha < 2\pi \right.}$$
(4.39)

Similarly, once the duration of the seventh operating stage depends on the output voltage of the converter, Δt_{7} (a) is defined as given by (4.40).

$$\Delta t_{7}(\alpha) = \begin{vmatrix} \frac{L_{G}I_{L1}(\alpha)}{V_{IN} + \frac{V_{0}(\alpha)}{n}} \rightarrow 0 < \alpha < \pi \\ \frac{L_{G}I_{L1}(\alpha)}{V_{IN} - \frac{V_{0}(\alpha)}{n}} \rightarrow \pi < \alpha < 2\pi \end{vmatrix}$$
(4.40)

As soon as the duration of the operating stages and the values of the currents I_{L1} (α) and I_{L2} (α) are known, it is possible to calculate the average and RMS current values for all components of the converter.

Figure 125 presents the waveform of the current in L_{g} during one switching period.

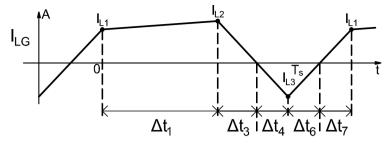


Figure 125 - Current waveform of the auxiliary switching inductor L_{g} . Source: Self-authorship

The average value of the current in the auxiliary switching inductor L_{g} during a period of the output voltage, is given by the integral equation (4.41).

$$I_{LG} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{(I_{L1}(\alpha) + I_{L2}(\alpha))\Delta t_{1}(\alpha) + (I_{L1}(\alpha) - I_{L2}(\alpha))(\Delta t_{6}(\alpha) + \Delta t_{7}(\alpha))}{2T_{s}} d\alpha \quad (4.41)$$

The RMS current value in L_{G} is derived from equation (4.42).

$$I_{LG_{-RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{A+B+C}{3T_{s}} d\alpha}$$
(4.42)

Where:

•
$$A = \left(I_{L1}(\alpha)^2 + I_{L1}(\alpha)I_{L2}(\alpha) + I_{L2}(\alpha)^2\right)\Delta t_1(\alpha);$$

• $B = I_{L2}(\alpha)\left(\Delta t_3(\alpha) + \Delta t_4(\alpha)\right);$
• $C = \left(I_{L1}(\alpha)^2 - I_{L1}(\alpha)I_{L2}(\alpha) + I_{L2}(\alpha)^2\right)\left(\Delta t_6(\alpha) + \Delta t_7(\alpha)\right)$

The maximum voltage over L_{g} , as previously presented in Figure 124, is given by (4.43) when $\alpha = \frac{\pi}{2}$ and $\alpha = \frac{3\pi}{2}$.

$$V_{LG_{max}} = V_{IN} + \frac{V_0(\alpha)}{n}$$
 (4.43)

6 | MAGNETIZING INDUCTANCE (LM)

The value of the magnetizing inductance is obtained from the inductance factor presented in (4.17). Considering that this analysis is based on the continuous conduction mode and that the current ripple in the magnetizing inductance is a design requirement, the current ripple on *LM* is confirmed when $\alpha = \frac{\pi}{2}$ and $\alpha = \frac{3\pi}{2}$ by means of (4.44).

$$\Delta I_{LM} \% = \frac{2(I_{L2}(\alpha) - I_{L2}(\alpha))}{I_{L1}(\alpha) + I_{L2}(\alpha)} 100$$
(4.44)

On solving the integral equation on (4.45), one can determine the average value of the current $I_{_{LM}}$.

$$I_{LM} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{I_{L1}(\alpha) + I_{L2}(\alpha)}{2} d\alpha$$
(4.45)

The RMS value of the current in the magnetizing inductance is derived from (4.46).

$$I_{LM_{-RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \left[\frac{I_{L1}(\alpha) + I_{L2}(\alpha)}{2} \right]^{2} d\alpha}$$
(4.46)

The voltage on the magnetizing inductance reaches its maximum value during the first operating stage when $\alpha = \pi/2$ and $\alpha = 3\pi/2$. Therefore, regardless of which semi-cycle the output voltage is on, the maximum voltage is obtained by the relation presented in (4.47).

$$V_{LM_{max}} = V_{IN} - V_{LG} (\Delta t_1)$$
(4.47)

7 | AUXILIARY SWITCHING CAPACITOR (CG)

The method adopted to calculate the auxiliary switching capacitor does not take into account the resonance that the capacitor has with the magnetizing and auxiliary inductances during the third and fourth operating stages. Instead, this resonance is considered a voltage ripple, presented as an initial design requirement. Therefore, the auxiliary switching capacitor presents a certain voltage ripple and its value is calculated to satisfy this requirement. It is noteworthy that the voltage ripple in the capacitor *CG* is considered negative because the voltage defined by (4.30) is negative as well. Therefore, considering that the voltage ripple is not a negative value, the convention presented in (4.48) was adopted.

$$\Delta V_{CG} = -V_{CG} \Delta V_{CG\%} \tag{4.48}$$

The equation that defines the capacitor by its voltage ripple is obtained from analysis of the current in the capacitor during the third operating stage, as equation (4.49) presents.

$$C_G = \frac{I_{L2}\Delta t_3}{2\Delta V_{CG}} \tag{4.49}$$

Based on the waveform of the current in the auxiliary switching capacitor $C_{_{G}}$, presented in Figure 126, both the average and RMS current values are determined by the integral equations presented in (4.50) and (4.51), respectively.

$$I_{CG} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{-I_{L2}(\alpha) \left(\Delta t_3(\alpha) - \Delta t_4(\alpha)\right)}{2T_s} d\alpha$$
(4.50)

$$I_{CG_{RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{I_{L2}(\alpha)^{2} (\Delta t_{3}(\alpha) + \Delta t_{4}(\alpha))}{3T_{s}}} d\alpha$$
(4.51)

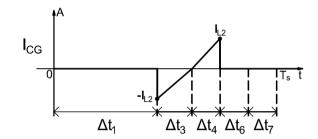


Figure 126 – Active-clamping flyback converter – current waveform in C_{g} . Source: Self-authorship

8 | MAIN SWITCH (S1)

The analysis of the waveform of the current in S_{η} , presented in Figure 127, shows that S_{η} has the same current values of I_{LG} during the first, sixth and seventh operating stages.

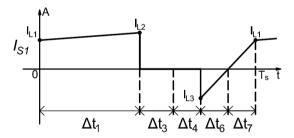


Figure 127 – Active-clamping flyback converter - current waveform in S_{ij} . Source: Self-authorship

This definition allows the evaluation of the average current in S_{i} as presented in (4.52).

$$I_{s_{1}} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{L_{1}}(\alpha) + I_{L_{2}}(\alpha)\right) \Delta t_{1}(\alpha) + \left(I_{L_{1}}(\alpha) - I_{L_{2}}(\alpha)\right) \left(\Delta t_{6}(\alpha) + \Delta t_{7}(\alpha)\right)}{2T_{s}} d\alpha \quad (4.52)$$

Equation (4.53) provides the means for calculating the RMS current value in S_{γ} .

$$I_{S1_{RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left[I_{L1}(\alpha) + I_{L2}(\alpha)\right]^{2} \Delta t_{1}(\alpha) + \left[I_{L1}(\alpha) - I_{L2}(\alpha)\right]^{2} \left(\Delta t_{6}(\alpha) + \Delta t_{7}(\alpha)\right)}{3T_{s}} d\alpha}$$

(4.53)

As presented in Figure 128, the maximum voltage across S_1 is $V_{Simax} = V_{IN} - V_{CG}$

ZVS is achieved in the main switch (S_{i}), when the PWM pulse of the switch is delayed from the exact moment when the sixth operating stage starts to a maximum moment when this operating stage finishes. Because the current is negative during the sixth operating stage, if the PWM pulse is not active, the current will circulate through the anti-parallel diode of the switch, which guarantees zero voltage over the terminals of the switch. In Figure 128, the hatched area shows that at any time during the sixth operating stage the voltage on S_{i} is already null, which guarantees the zero voltage switching. However, if the PWM pulse is not given until the sixth stage finishes, the seventh operating stage will not start.

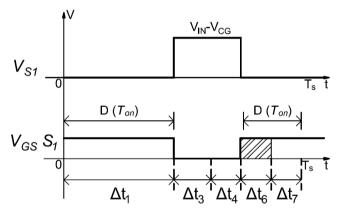


Figure 128 – Active-clamping flyback converter – voltage waveform in S_{i} . Source: Self-authorship

9 | AUXILIARY ACTIVE-CLAMPING SWITCH (SG)

Considering the equivalent circuit of the third and fourth operating stages (respectively, Figure 119 and Figure 120) when $C_{_G}$ and $S_{_G}$ are associated in series, the current that circulates in the auxiliary active-clamping switch is the same as the auxiliary switching capacitor. Therefore, the equations of the average and effective current values for $S_{_G}$ are the same as presented for the auxiliary switching capacitor, respectively in (4.50) and (4.51).

Similar to the main switch S_{η} , ZVS is achieved in S_{G} by delaying the command pulse to the switch. In this case, the current in the switch is negative during the third operating stage (Figure 126), which means that the pulse can be delayed for as long as the third

operating stage endures. Therefore, the switch must be turned on in order to start the fourth operating stage.

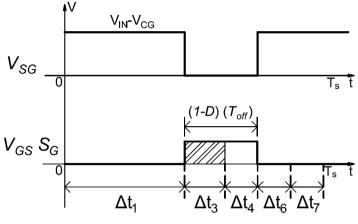


Figure 129 - Active-clamping flyback converter – voltage waveform in S_{i} . Source: Self-authorship

Ideally, the PWM pulse is delayed for a short while because the on resistance (R_{DSon}) of the switch is smaller than the intrinsic resistance of the anti-parallel diode in the switch, thus reducing the conduction losses. In addition, by turning on the switch, the voltage drop of the anti-parallel diode is taken out of equation.

10 I OUTPUT FILTER CAPACITOR (C_{o})

The choice of the output filter capacitor is made under the same premises of the auxiliary switching capacitor. A voltage ripple is defined as an initial design requirement based on the output voltage of the converter and the capacitor is then defined in order to satisfy this requirement. The output voltage ripple is defined as given by (4.54).

$$\Delta V_0 = V_0 \Delta V_{0\%} \tag{4.54}$$

The equation of the output capacitor by its voltage ripple is determined for the duration of the duty cycle of the main switch (D), where the output capacitor discharges, supplying the current to the output, as presented in (4.55).

$$C_0 = \frac{I_0 D}{\Delta V_0 f_s} \tag{4.55}$$

11 I BLOCKING DIODES (D_p AND D_n) AND SWITCHES (S_p AND S_n)

 $I_{DP}\left(\frac{\pi}{2}\right) = I_{DN}\left(\frac{3\pi}{2}\right) = \frac{I_{L2} + I_{LX}}{n}$

Voltages and currents for both diodes D_p and D_N present the same value, though the operation of these diodes occur in distinct periods. When the angle a varies from zero to p (*pi*), the energy is transferred from the primary to the secondary winding of the flyback inductor through D_p . Similarly, whena varies from π to 2π the energy is transferred through D_N . Therefore, even though the waveform of the current presented in Figure 130 is identified as I_{Dp} it is valid for the analysis of the current in D_N when $V_q < 0$ and $\pi < \alpha < 2\pi$.

The maximum current in both D_P and $D_{N'}$ presented in Figure 130, is given by (4.56).

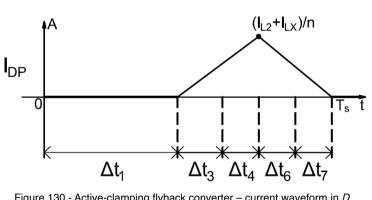


Figure 130 - Active-clamping flyback converter – current waveform in D_p. Source: Self-authorship

The average current value is calculated as given by the integral equation (4.57) for D_P and as (4.58) for D_N Because one diode is conducting while the other is blocked for half a cycle of the output current, D_P is turned on from $0 < \alpha < \pi$, while D_N is turned on from $\pi < \alpha < 2\pi$.

$$I_{DP} = \frac{1}{2\pi} \int_{0}^{\pi} \frac{\left(I_{LX}\left(\alpha\right) + I_{L2}\left(\alpha\right)\right) \left(\Delta t_{3}\left(\alpha\right) + \Delta t_{4}\left(\alpha\right) + \Delta t_{6}\left(\alpha\right) + \Delta t_{7}\left(\alpha\right)\right)}{2T_{s}n} d\alpha \qquad (4.57)$$

$$I_{DN} = \frac{1}{2\pi} \int_{\pi}^{2\pi} \frac{\left(I_{LX}\left(\alpha\right) + I_{L2}\left(\alpha\right)\right) \left(\Delta t_{3}\left(\alpha\right) + \Delta t_{4}\left(\alpha\right) + \Delta t_{6}\left(\alpha\right) + \Delta t_{7}\left(\alpha\right)\right)}{2T_{s}n} d\alpha \qquad (4.58)$$

The RMS currents values in D_{P} and D_{N} are obtained by solving (4.59) and (4.60), respectively.

(4.56)

$$I_{DP_{-RMS}} = \sqrt{\frac{1}{2\pi} \int_{0}^{\pi} \frac{\left(I_{LX}\left(\alpha\right) + I_{L2}\left(\alpha\right)\right)^{2} \left(\Delta t_{3}\left(\alpha\right) + \Delta t_{4}\left(\alpha\right) + \Delta t_{6}\left(\alpha\right) + \Delta t_{7}\left(\alpha\right)\right)}{3T_{s}n^{2}} d\alpha} \quad (4.59)$$

$$I_{DN_{-RMS}} = \sqrt{\frac{1}{2\pi} \int_{\pi}^{2\pi} \frac{\left(I_{LX}\left(\alpha\right) + I_{L2}\left(\alpha\right)\right)^{2} \left(\Delta t_{3}\left(\alpha\right) + \Delta t_{4}\left(\alpha\right) + \Delta t_{6}\left(\alpha\right) + \Delta t_{7}\left(\alpha\right)\right)}{3T_{s}n^{2}} d\alpha \quad (4.60)$$

The maximum voltage on DP and DN are defined, respectively, by (4.61) and (4.62).

$$V_{DP_{-}\max} = V_0 \left(\frac{\pi}{2}\right) + V_0 \left(\frac{\pi}{2}\right) \Delta V_{0\%} + V_{LM} n$$
(4.61)

$$V_{DN_{max}} = -V_0 \left(\frac{3\pi}{2}\right) - V_0 \left(\frac{3\pi}{2}\right) \Delta V_{0\%} + V_{LM} n$$
(4.62)

Because the blocking diodes are positioned in series with switches S_p and S_N , and the switching strategy states that switch and diode are turned on at the same time, the current in both switches are the same as the diode in which they are is in series with. Therefore, the average current in S_p is the same as D_p and S_N the same as D_N , as respectively given by (4.63) and (4.64).

$$I_{DP} = I_{SP} \tag{4.63}$$

$$I_{DN} = I_{SN} \tag{4.64}$$

Similarly, the RMS current values are the same as well, as (4.65) and (4.66) present.

$$I_{SP_RMS} = I_{DP_RMS}$$
(4.65)

$$I_{SN_RMS} = I_{DN_RMS}$$
(4.66)

Maximum voltage on S_{p} happens when, in the negative semi-cycle, the output and magnetizing inductance voltages sum on its terminals at $\alpha = {}^{3}\pi/_{2}$, as given by (4.67). The same situation occurs in the positive semi-cycle for S_{N} when $\alpha = \pi/_{2}$, as presented in (4.68)

$$V_{SP_{max}} = -V_{LM}n - V_0\left(\frac{3\pi}{2}\right)$$
(4.67)

$$V_{SN_{max}} = -V_{LM}n - V_0\left(\frac{\pi}{2}\right)$$
 (4.68)

12 I SMALL-SIGNAL ANALYSIS WITH RESISTIVE OUTPUT LOAD

A simplified model is proposed for the small signal analysis of the converter, so that the current in the magnetizing inductance is considered constant. This simplification changes the variation of the current in the auxiliary switching inductance during the first operating stage as well. Therefore, the operating stages must be reanalyzed and I_{LM} must be redefined. Figure 131 shows the difference of the current analyzed in the model adopted (A) up until this point and the simplified model (B). This analysis, although simplified, presents high fidelity in relation to the behavior of the converter.

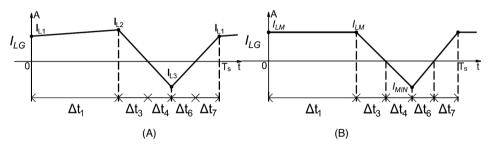


Figure 131 - Active-clamping flyback converter waveform of the current in L_G in (A) adopted model. (B) Simplified model.

Source: Self-authorship

The equivalent circuits of the operating stages remain the same. However, based on the differences of the waveforms presented in Figure 131 (A) and Figure 131 (B), the initial and final conditions of each operating stage must be reassessed.

In the first operating stage, there is no variation of the current in L_{g} . Therefore, the voltage V_{LG} is zero.

During the third operating stage, the current in L_{G} varies from I_{LM} to zero. From the analysis of the equivalent circuit (Figure 119), the voltage on L_{G} is defined by (4.70). The duration of the third operating stage is obtained from the Faraday's law of induction, which gives (4.70).

$$V_{LG} = -V_{CG} + \frac{V_0}{n}$$
(4.69)

$$\Delta t_3 = \frac{I_{LM} L_G}{\left(V_{CG} - \frac{V_0}{n}\right)} \tag{4.70}$$

The current in the auxiliary switching inductance changes from zero to $-I_{_{MIN}}$ in the fourth operating stage. The analysis of the voltages in this operating stage, on the other hand, shows that there is no variation of the equivalent circuit, as (4.71) presents. The

duration of the fourth operating stage is given by (4.72).

$$V_{LG} = -V_{CG} + \frac{V_0}{n}$$
(4.71)

$$\Delta t_4 = \frac{I_{MIN} L_G}{V_{CG} - \frac{V_0}{n}}$$
(4.72)

In the sixth operating stage, as $S_{_{1P}}$ is turned on, the equivalent circuit changes in relation to the fourth operating stage. In addition, the current changes from $-I_{_{MIN}}$ to zero. The voltage on $L_{_{G'}}$ obtained from the analysis of the equivalent circuit, is presented in (4.73). The duration of the sixth operating stage is given by (4.74).

$$V_{LG} = V_{IN} + \frac{V_0}{n}$$
(4.73)

$$\Delta t_6 = \frac{I_{MIN}L_G}{E + \frac{V_0}{n}} \tag{4.74}$$

Finally, the current in L_{G} changes from zero to I_{LM} in the seventh operating stage. Because the equivalent circuit does not change from the sixth to the seventh operating stage, the voltage on L_{G} does not change from the previous stage, as (4.75) shows. The duration of the seventh operating stage is given by (4.76).

$$V_{LG} = V_{IN} + \frac{V_0}{n}$$
(4.75)

$$\Delta t_{7} = \frac{I_{LM} L_{G}}{V_{IN} + \frac{V_{0}}{n}}$$
(4.76)

Assuming that, the duration of the third and fourth operating stages are equal in steady state and that these two operating stages correspond to the off period of S_{i} , Δt_{3} and Δt_{4} can be defined as given by (4.77).

$$\Delta t_3 = \Delta t_4 = \frac{(1-D)}{2f_s}$$
(4.77)

Once an additional equation defines both Δt_3 and Δt_4 in (4.77), the average current values for I_{LM} and I_{MIN} are obtained, respectively, from (4.70) and (4.72), as given by (4.78) and (4.79), respectively.

$$I_{LM} = \frac{(1-D)\left(V_{CG} - \frac{V_0}{n}\right)}{2f_s L_G}$$
(4.78)

$$I_{MIN} = \frac{(1-D)\left(V_{CG} - \frac{V_0}{n}\right)}{2f_s L_G}$$
(4.79)

The resultant equations (4.78) and (4.79) indicate that since the duration of the third and fourth operating stages are set as equal in (4.77), I_{LM} and I_{MIN} are equal as well. By substituting (4.79) in (4.74) an equation that defines Δt_6 is defined without depending on I_{MIN} as given by (4.80).

$$\Delta t_{6} = \frac{(1-D)\left(V_{CG} - \frac{V_{0}}{n}\right)}{2f_{s}\left(V_{IN} + \frac{V_{0}}{n}\right)}$$
(4.80)

Similarly, by substituting (4.78) in (4.76), an equation that defines Δt_7 without depending on I_{1M} is given by (4.81).

$$\Delta t_{7} = \frac{(1-D)\left(V_{CG} - \frac{V_{0}}{n}\right)}{2f_{s}\left(V_{IN} + \frac{V_{0}}{n}\right)}$$
(4.81)

Considering that switch S_{i} is turned on during the first, sixth and seventh operating stages, the duration of the first operating stage is finally obtained from the sum of the operating stages that consist the duty cycle. Thus, Δt_{i} is given by (4.82).

$$\Delta t_{1} = \frac{D}{f_{s}} - \frac{(1-D)\left(V_{CG} - \frac{V_{0}}{n}\right)}{f_{s}\left(V_{IN} + \frac{V_{0}}{n}\right)}$$
(4.82)

As the equivalent circuits of the operating stages are the same as presented in section 4.3, the voltage V_{CG} , obtained from the volt-second analysis of the magnetizing inductance L_{M} is the same as (4.30).

Despite the assumption of the third and fourth operating stages being equal with the converter operating in steady state, this equality is not true for a transient response. Therefore, different equations that define I_{MIN} and Δt_4 are needed for further linearization. In this case, Δt_4 can be defined as given by (4.83).

$$\Delta t_4 = \frac{1 - D}{f_s} - \frac{I_{LM} L_G}{V_{CG} - \frac{V_0}{n}}$$
(4.83)

By substituting (4.83) in (4.72), I_{MIN} is defined as presented in (4.84).

$$I_{MIN} = \frac{\left(V_{CG} - \frac{V_0}{n}\right)(1 - D)}{f_s L_G} - I_{LM}$$
(4.84)

It is noteworthy that (4.83) and (4.84) are not equal to (4.77) and (4.79), respectively, unless they are forced to be.

The small-signal variation of $I_{_{MIN}}$ is obtained by applying perturbations in (4.84), as given by the resultant first order terms presented in (4.85).

$$\hat{i}_{\min}(t) = \frac{-\hat{d}(t)\left(V_{CG} - \frac{V_0}{n}\right)}{f_s L_G} + \frac{\hat{v}_{CG}(t)D'}{f_s L_G} - \frac{\hat{v}_0(t)D'}{nf_s L_G} - \hat{i}_{LM}(t)$$
(4.85)

Next, the linearization of the duration of the operating stages are necessary, in order to obtain the control to output transfer function. The linearization of obtained by applying the partial differentiations presented in (4.86).

$$\hat{\Delta t}_{3}(t) = \frac{\partial \Delta t_{3}}{\partial V_{0}} \hat{v}_{0}(t) + \frac{\partial \Delta t_{3}}{\partial I_{LM}} \hat{i}_{LM}(t) + \frac{\partial \Delta t_{3}}{\partial V_{CG}} \hat{v}_{CG}(t)$$
(4.86)

Using equation (4.70) in (4.86), Δt_{3} (*t*) is given by (4.87).

$$\hat{\Delta t}_{3}(t) = \frac{I_{LM}L_{G}}{n\left(V_{CG} - \frac{V_{0}}{n}\right)^{2}} \hat{v}_{0}(t) + \frac{L_{G}}{\left(V_{CG} - \frac{V_{0}}{n}\right)} \hat{i}_{LM}(t) - \frac{I_{LM}L_{G}}{\left(V_{CG} - \frac{V_{0}}{n}\right)^{2}} \hat{v}_{CG}(t) \quad (4.87)$$

The linearization of Δt_4 is given by (4.88).

$$\hat{\Delta t}_{4}(t) = \frac{\partial \Delta t_{4}}{\partial D} \hat{d}(t) + \frac{\partial \Delta t_{4}}{\partial V_{CG}} \hat{v}_{CG}(t) + \frac{\partial \Delta t_{4}}{\partial V_{0}} \hat{v}_{o}(t) + \frac{\partial \Delta t_{4}}{\partial I_{LM}} \hat{i}_{LM}(t)$$
(4.88)

Using equation (4.83) in (4.88), $\hat{\Delta t}_4(t)$ is obtained as given by (4.89).

$$\hat{\Delta t}_{4}(t) = -\hat{d}(t)\frac{1}{f_{s}} + \frac{I_{LM}L_{G}}{\left(V_{CG} - \frac{V_{0}}{n}\right)^{2}}\hat{v}_{CG}(t) - \frac{I_{LM}L_{G}}{n\left(V_{CG} - \frac{V_{0}}{n}\right)^{2}}\hat{v}_{0}(t) - \frac{L_{G}}{V_{CG} - \frac{V_{0}}{n}}\hat{i}_{LM}(t)$$
(4.89)

The linearization of Δt_6 is given by (4.90).

$$\hat{\Delta t}_{6}(t) = \frac{\partial \Delta t_{6}}{\partial V_{CG}} \hat{v}_{CG}(t) + \frac{\partial \Delta t_{6}}{\partial V_{0}} \hat{v}_{0}(t) + \frac{\partial \Delta t_{6}}{\partial I_{LM}} \hat{i}_{LM}(t) + \frac{\partial \Delta t_{6}}{\partial D} \hat{d}(t)$$
(4.90)

Using (4.74) in (4.90), $\hat{\Delta t}_{6}(t)$ is given by (4.91).

$$\hat{\Delta t}_{6}(t) = -\frac{(1-D)(V_{IN}+V_{CG})-I_{LM}f_{s}L_{G}}{f_{s}\left(V_{IN}+V_{0}^{\prime}\right)^{2}}v_{0}(t) + \frac{(1-D)}{f_{s}\left(V_{IN}+V_{0}^{\prime}\right)}v_{CG}(t) - \frac{\left(V_{CG}-V_{0}^{\prime}\right)}{f_{s}\left(V_{IN}+V_{0}^{\prime}\right)}\hat{d}(t) - \frac{L_{G}}{\left(V_{IN}+V_{0}^{\prime}\right)}\hat{t}_{LM}(t)$$

$$(4.91)$$

The linearization of Δt_7 is given by (4.92).

$$\hat{\Delta t}_{7}(t) = \frac{\partial \Delta t_{7}}{\partial V_{0}} \hat{v}_{0}(t) + \frac{\partial \Delta t_{7}}{\partial I_{LM}} \hat{i}_{LM}(t)$$
(4.92)

Using (4.76) in (4.92), $\hat{\Delta t}_7(t)$ is given by (4.93).

$$\hat{\Delta t}_{7}(t) = \frac{-I_{LM}L_{G}}{n\left(V_{IN} + \frac{V_{0}}{n}\right)^{2}} \hat{v}_{0}(t) + \frac{LG}{V_{IN} + \frac{V_{0}}{n}} \hat{i}_{LM}(t)$$
(4.93)

The linearization of Δt_1 is obtained by equation (4.94).

$$\hat{\Delta t}_{1}(t) = \frac{\hat{d}(t)}{f_{s}} - \hat{\Delta t}_{6}(t) - \hat{\Delta t}_{7}(t)$$
(4.94)

Using (4.91) and (4.93) in (4.94), $\hat{\Delta t}_1$ (*t*) is given by (4.95).

$$\hat{\Delta t}_{1}(t) = \frac{V_{IN} + V_{CG}}{f_{s} \left(V_{IN} + \frac{V_{0}}{n} \right)} \hat{d}(t) + \frac{(1-D)(E+V_{CG})}{f_{s} \left(V_{IN} + \frac{V_{0}}{n} \right)^{2} n} \hat{v}_{0}(t) - \frac{(1-D)}{f_{s} \left(V_{IN} + \frac{V_{0}}{n} \right)} \hat{v}_{CG}(t) \quad (4.95)$$

With the duration of all the operating stages already linearized, it is necessary to apply the volt-second balance in the magnetizing inductance, which reads as given by equation (4.96).

$$L_{M}\left(\frac{dI_{LM}}{dt} + \frac{\dot{di_{LM}}(t)}{dt}\right) = \left(\Delta t_{1} + \dot{\Delta t}_{1}(t)\right)\left(V_{IN} + \dot{v}_{IN}(t)\right) + \left(\frac{1}{f_{s}} - \Delta t_{1} - \dot{\Delta t}_{1}(t)\right)\left(-\frac{\dot{v}_{0}(t)}{n} - \frac{\dot{v}_{0}(t)}{n}\right)$$

$$(4.96)$$

The first order terms of equation (4.96) are used to apply the Laplace transform and to obtain (4.97).

$$sL_{M} i_{LM}(s) = \Delta t_{1}(s) f_{s} \left(V_{IN} + \frac{V_{0}}{n} \right) - \frac{v_{0}(s)}{n} (1 - \Delta t_{1} f_{s})$$
(4.97)

Next, the capacitor charge balance in $C_{G'}$ is given by equation (4.98).

$$C_{G}\left(\frac{dV_{CG}}{dt} + \frac{d\dot{v_{CG}}(t)}{dt}\right) = \left(\Delta t_{3} + \dot{\Delta t_{3}}(t)\right) \left(\frac{I_{LM}}{2} + \frac{\dot{i_{LM}}(t)}{2}\right) f_{s} - \left(\Delta t_{4} + \dot{\Delta t_{4}}(t)\right) \left(\frac{I_{MIN}}{2} + \frac{\dot{i_{MIN}}(t)}{2}\right) f_{s}$$

$$(4.98)$$

The first order terms of (4.98) are used to apply the Laplace transform and obtain (4.99).

$$sC_{G}v_{CG}(t) = \Delta t_{3}\frac{\dot{i_{LM}}(s)}{2}f_{s} + \dot{\Delta t_{3}}(s)\frac{I_{LM}}{2}f_{s} - \Delta t_{4}\frac{\dot{i_{\min}}(s)}{2}f_{s} - \dot{\Delta t_{4}}(s)\frac{I_{MIN}}{2}f_{s}$$
(4.99)

Finally, the last frequency domain equation is obtained, initially, from the analysis of the current in the diode, which is given by (4.100).

$$\langle i_{DP} \rangle = f_s \left(\frac{1}{f_s} - \Delta t_1 \right) \left(\frac{I_{LM} + I_{MIN}}{2} \right)$$
 (4.100)

From the sum of currents in the output filter capacitor, it is possible to obtain (4.101).

$$\langle i_{CO} \rangle = \langle i_{DP} \rangle - \langle i_0 \rangle$$
 (4.101)

Use (4.100) in (4.101) and perturb, to obtain (4.102).

$$C_{0}\left[\frac{dV_{0}}{dt} + \frac{d\dot{v_{0}}(t)}{dt}\right] = f_{s}\left(\frac{1}{f_{s}} - \Delta t_{1} - \dot{\Delta t_{1}}(t)\right)\left(\frac{I_{LM} + I_{MIN}}{2} + \frac{\dot{i_{LM}}(t) + \dot{i_{MIN}}(t)}{2}\right) - \frac{V_{0}}{R} - \frac{\dot{v_{0}}(t)}{R}$$
(4.102)

The Laplace transform of the resulting first order terms from (4.102) results in (4.103).

$$sC_{0}\hat{v}_{0}(s) = \frac{f_{s}}{2n} \left(\hat{i}_{LM}(s) + \hat{i}_{MIN}(s) \right) - \frac{\Delta t_{1}f_{s}}{2n} \left(\hat{i}_{LM}(s) + \hat{i}_{MIN}(s) \right) - \frac{\Delta t_{1}(s)f_{s}}{2n} \left(I_{LM} + I_{MIN} \right) - \frac{\hat{v}_{0}}{R}$$
(4.103)

With equations (4.97), (4.99) and (4.103) a system of equations is built in (4.104) that shows two unknown variables in $i_{LM}^{\circ}(s)$ and $v_{CG}^{\circ}(s)$.

$$\begin{cases} sL_{M} \hat{i}_{LM}(s) = \Delta t_{1}(s) f_{s} \left(V_{IN} + \frac{V_{0}}{n} \right) - \frac{\hat{v}_{0}(s)}{n} (1 - \Delta t_{1} f_{s}) \\ sC_{G} \hat{v}_{CG}(t) = \Delta t_{3} \frac{\hat{i}_{LM}(s)}{2} f_{s} + \Delta t_{3}(s) \frac{I_{LM}}{2} f_{s} - \Delta t_{4} \frac{\hat{i}_{\min}(s)}{2} f_{s} - \Delta t_{4} (s) \frac{I_{MIN}}{2} f_{s} \\ sC_{0} \hat{v}_{0}(s) = \frac{f_{s}}{2n} \left(\hat{i}_{LM}(s) + \hat{i}_{MIN}(s) \right) - \frac{\Delta t_{1} f_{s}}{2n} \left(\hat{i}_{LM}(s) + \hat{i}_{MIN}(s) \right) - \frac{\Delta t_{1} f_{s}}{2n} \left(\hat{i}_{LM}(s) + \hat{i}_{MIN}(s) \right) - \frac{\Delta t_{1} f_{s}}{2n} \left(\hat{i}_{LM}(s) + \hat{i}_{MIN}(s) \right) - \frac{\Delta t_{1} (s) f_{s}}{2n} (I_{LM} + I_{MIN}) - \frac{\hat{v}_{0}}{R} \end{cases}$$

$$(4.104)$$

Substitute $v'_{0}(s)$ for $i'_{0}(s) R_{0}$ to obtain the system of equations presented in

$$\begin{cases} sL_{M} \ \hat{i}_{LM}(s) = \hat{\Delta t}_{1}(s) \ f_{s}\left(V_{IN} + \frac{V_{0}}{n}\right) - \frac{\hat{i}_{0}(s) R_{0}}{n} (1 - \Delta t_{1} f_{s}) \\ sC_{G} \ \hat{v}_{CG}(t) = \Delta t_{3} \frac{\hat{i}_{LM}(s)}{2} \ f_{s} + \hat{\Delta t}_{3}(s) \frac{I_{LM}}{2} \ f_{s} - \Delta t_{4} \frac{\hat{i}_{\min}(s)}{2} \ f_{s} - \hat{\Delta t}_{4}(s) \frac{I_{MN}}{2} \ f_{s} \\ sC_{0} \ \hat{i}_{0}(s) R_{0} = \frac{f_{s}}{2n} \left(\hat{i}_{LM}(s) + \hat{i}_{MIN}(s)\right) - \frac{\Delta t_{1} f_{s}}{2n} \left(\hat{i}_{LM}(s) + \hat{i}_{MIN}(s)\right) - \frac{\hat{\Delta t}_{1}(s) f_{s}}{2n} (I_{LM} + I_{MIN}) - \hat{i}_{0}(s) \end{cases}$$

$$(4.105)$$

By substituting the small-signal variables of the duration of the operating stages and isolating the unknown variables, the duty-cycle-to-output-current transfer function is obtained as given by (4.106).

$$\frac{\dot{i}_{0}(s)}{\dot{d}(s)} = \frac{B_{3}s^{3} + B_{2}s^{2} + B_{1}s + B_{0}s}{A_{3}s^{3} + A_{2}s^{2} + A_{1}s + A_{0}}$$
(4.106)

Where:

• $B_3 = 0$;

•
$$B_2 = 8C_G L_G L_M f_s n (nV_{CG} - V_0) (V_{IN} + V_{CG}) (nV_{IN} + V_0) (-1 + D);$$

•
$$B_1 = 2L_M (-1+D)^3 (nV_{IN}+V_0)^2 (nV_{CG}-V_0)$$
;

• $B_0 = -4 f_s n L_G (-1 + D)^3 (n V_{IN} + V_0)^2 (V_{IN} + V_{CG})$;

•
$$A_3 = 8C_G C_0 L_G^2 L_M R_0 f_s^2 n^2 (nV_{IN} + V_0)^2$$

•
$$A_2 = 8n^2 f_s L_G L_M [A_{201} + A_{202}];$$

 $A_{201} = \left[\left[\frac{1}{2} (n^2 C_0 + C_G) V_{IN}^2 + (2C_0 V_0 n + 2C_G V_{CG}) V_{IN} + V_{CG}^2 C_G + V_0^2 C_0 \right] (-1 + D)^2 R_0 \right]$
 $A_{202} = f_s L_G C_G (n V_{IN} + V_0)^2;$

•
$$A_{1} = 8(-1+D)^{2} \Big[A_{101} + R_{0}n^{2}C_{0}L_{G}^{2}f_{s}^{2}(nV_{IN}+V_{0})^{2} \Big]$$

 $A_{101} = \Big[\frac{1}{4} (-1+D)^{2} (nV_{CG}-V_{0})^{2}R_{0} + \frac{1}{2}n^{2}L_{G}f_{s}(nV_{IN}+V_{0})^{2} \Big] L_{M}$;
• $A_{0} = 4n^{2}f_{s}L_{G} \Big[(-1+D)^{2} (V_{IN}+V_{CG})^{2}R_{0} + 2L_{G}f_{s}(nV_{IN}+V_{0})^{2} \Big] (-1+D)^{2}$.

13 | CONCLUSION

This chapter presents a dc-ac active-clamping flyback converter that offers some improvements from the converter previously studied in Chapters 2 and 3. Also, a mathematical analysis of the currents and voltages in all components are studied in depth. Some simplifications were made concerning the voltage and current in the auxiliary switching capacitor CG, whose impacts are evaluated in the simulation and experimental results in Chapter 5. In addition, a duty-cycle-to-output-current transfer function is presented for an offline, linear load application.

DESIGN, SIMULATION AND EXPERIMENTAL RESULTS OF THE DC-AC ACTIVE CLAMPING FLYBACK CONVERTER

1 | INTRODUCTION

This chapter presents the design of the prototype based on the converter analyzed in Chapter 4. Initially, a methodology is proposed for the design of the prototype, in order to determine and satisfy the design requirements. The calculated values in the design methodology are confirmed by means of numerical simulation. Finally, experimental results are presented.

2 I DESIGN METHODOLOGY

Table 13 presents the initial design requirements chosen for this methodology.

Input Voltage	E
RMS Output Voltage	V _{0_RMS}
Output Voltage Frequency	f _r
Active Output Power	P _o
Switching Frequency	f _s
Coupled Inductor Current Ripple	ΔI_{L}
Voltage Conversion Ratio	М

Table 13 - Requirements of the DC-AC active-clamping flyback converter. Source: Self-authorship

Once the requirements are known, one can follow the steps of the script below to design the converter:

- · Determine a maximum output voltage, based on the RMS output voltage value;
- Calculate the equivalent turns ratio of the flyback inductor for the given static gain;
- Determine a small auxiliary switching inductor (L_G) that guarantees soft- switching in S₁ and S_G;
- Calculate the equivalent parameterized output current;
- Calculate the maximum duty cycle and inductance factor;
- Calculate the maximum (I_{L1}) and minimum (I_{L2}) current in the magnetizing inductance;

- Calculate the magnetizing inductance (L_{M}) ;
- Calculate the auxiliary switching capacitance (C_G) in order to result in a small voltage ripple;
- · Calculate the duration of each operating stage;
- Calculate the average and RMS current values for the inductors, switches, diodes and capacitors;
- · Calculate the maximum voltage over the components of the circuit;
- Calculate the output capacitor (C_o) .

3 | REQUIREMENTS SPECIFICATIONS

For comparative purposes and similarity of applications, the rated output power, utility line frequency, input voltage and output voltage were maintained from the converter presented in Chapter 3.

The switching frequency was initially set at 100 kHz and the prototype was designed and optimized for this switching frequency. However, as the initial tests were performed, the concerns over the driver technology used in both prototypes presented in this work were confirmed and some of the switching losses verified were justified by the inability of the driver to trigger the gate of the switches fast enough. A speculative test with both an auxiliary switching inductance (L_{g}) and a magnetizing inductance (L_{M}) specially designed for 50 kHz was performed to check potential improvements.

Considering that the final purpose of this research is to design converters suited for grid connection applications, the current ripple in the magnetizing inductance was set as high as 30 % (*100 kHz*) and 50% (*50 kHz*) of the average current when $\alpha = \pi/2$ or when $\alpha = 3\pi/2$. This advantage allows reducing the magnetizing inductance value, therefore, reducing the volume of the magnetics. Grid-tied inverters, in order to reduce as much as possible the high frequency harmonics, usually have an additional high frequency choke at its output. This advantage allows high frequency harmonics to be filtered in the output instead of in the magnetizing inductance of the flyback inductor.

Considering the effects of voltage surges on the overall power efficiency of the converter presented in Chapter 3, the utilization of the turns ratio of the flyback inductor was preferred instead of using it for the sole purpose of galvanic isolation. This decision led to reduced voltage on the primary winding, therefore the voltage on the switches are reduced as well. Another advantageous fact is that the switches in the secondary windings are complementarily switched in the same frequency of the utility line, which means that the change of state occurs when the output voltage is almost zero.

Table 14 summarizes the requirements adopted for the design of the dc-ac activeclamping flyback converter.

Input Voltage	E	70 V
RMS Output Voltage	V _{o_RMS}	127 V
Output Voltage Frequency	f _r	60 Hz
Active Output Power	P _o	500 W
Switching Frequency	f _s	50 kHz / 100 kHz
Coupled Inductor Current Ripple	ΔΙ _L (50/100 kHz)	50 % / 30 %
Voltage Conversion Ratio	Μ	0.6

 Table 14 - Requirements specifications of the DC-AC active-clamping flyback converter.

 Source: Self-authorship

4 | NUMERICAL SIMULATION

This section presents the simulation results obtained. The value of the components used for both simulations are presented in Table 5, as a results of the calculations presented in Appendix G for the *50kHz* converter and Appendix H for the *100 kHz*.

The auxiliary switching inductance and current ripple in the magnetizing inductance were adjusted from the original *100 kHz* calculation in order to keep the parameterized output current, duty cycle and current values in the magnetizing inductance as close as possible when operating in *50 kHz*.

	Variable	50 kHz	100 kHz
Maximum Output Voltage	Vo	179.6 V	179.6 V
Turns Ratio	1:n	4.267	4.267
Auxiliary Switching Inductor	L _G	4 µF	2 µF
Parameterized Output Current	Ī	0.136	0.136
Maximum Duty Cycle	D	0.545	0.531
Inductance Factor	λ	0.153	0.09
Minimum Current in <i>LM</i>	<i>Ι_{LM1} (</i> π <i>2</i>)	28.571 A	32.381 A
Maximum Current in LM	I _{LM 2} (π 2)	47.619 A	43.81 A
Magnetizing Inductance	L _M	26.062 μH	22.219 µH
Auxiliary Switching Capacitance	C _G	2 µF	2 µF
Output Capacitor	C _o	2 µF	2 µF

Table 15 - DC-AC active-clamping flyback converter – calculated components.

Source: Self-authorship

The software PSIM® performed all simulation results presented in this chapter. Figure 132 presents the simulated circuit for both switching frequencies.

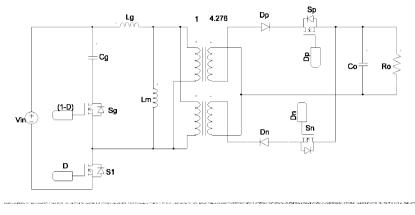


Figure 132 - Simulation circuit - DC-AC active-clamping flyback converter. Source: Self-authorship

The validation of the analysis, therefore the equations obtained, are performed here using the parameters calculated for the converter operating with switching frequency of 100 kHz.

Considering that the majority of the analysis depends on the accuracy of the values of I_{L1} and I_{L2} , the first two variables to be verified are these. Figure 133 presents the current in the magnetizing inductance (L_M) . The values of the maximum and minimum current in L_M are of singular importance because the equations that define the duration of the operating stages depend directly on them. In the waveform presented in Figure 133, the maximum current (I_{L2}) is 45.55 A and the minimum (I_{L1}) is 33.9 A. The differences from the calculated values to the simulated results are, respectively, of 3,97 % and 4.99 %. These differences are justified by the simplification made for the calculation of the currents and voltages, where the dynamics between C_G , L_M and L_G are neglected. Thus, these results are considered acceptable as long as the duration of the operating stages presents acceptable approximated values as well.

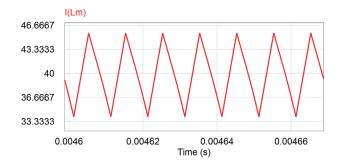
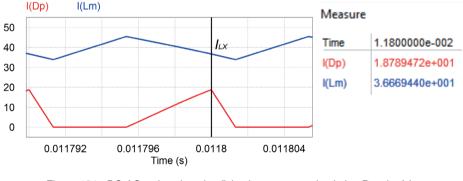


Figure 133 - DC-AC active-clamping flyback converter - simulation results of the L_{M} current. Source: Self-authorship

Another important value that validates the analysis of the converter is the intermediate current value I_{Lx} . Obtained from the variation of the current in the magnetizing inductance from I_{L2} to I_{L1} and used to define the current in the blocking diodes, given by (4.23), this value is important to define the duty cycle of the converter by means of the output current equation. Figure 134 presents the value of the current in the magnetizing inductance when the current is maximum in the blocking diode D_{p} . For $\alpha = \mathcal{V}_{2}$, the difference between the calculated and simulated value is 4.7%, which is within the differences obtained from the same comparison made for I_{L1} and I_{L2} .



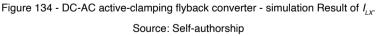
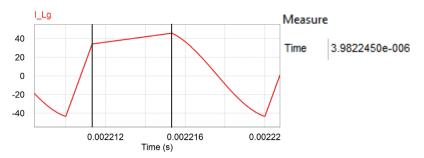


Figure 135 confirms the duration of the first operating stage given by equation (4.37) and the theoretical waveform presented in Figure 124. When $\alpha = \mathcal{V}_2$, a difference of 0.7 % is registered between calculations and simulation results.



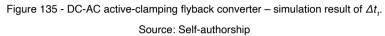
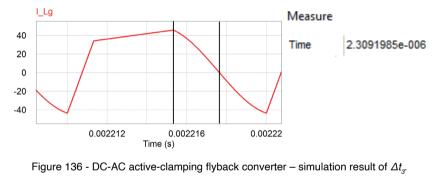
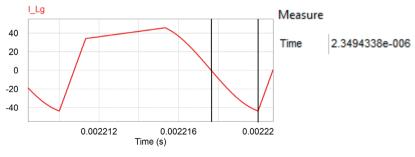


Figure 136 confirms the duration of the third operating stage given by equation (4.38). When $\alpha = \frac{\pi}{2}$, the difference between calculations and simulation results is *1.47%*.



Source: Self-authorship

Figure 137 confirms the duration of the fourth operating stage given by equation (4.38). When $\alpha = \frac{\pi}{2}$, the difference between calculations and simulation results is 0.2%.



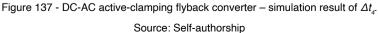


Figure 138 confirms the duration of the sixth operating stage given by equation (4.39). When $a = \frac{\eta_2}{2}$, the difference between calculations and simulation results is 4.7%.

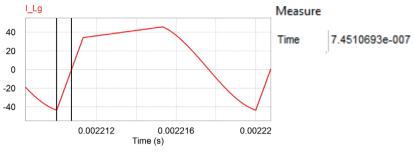
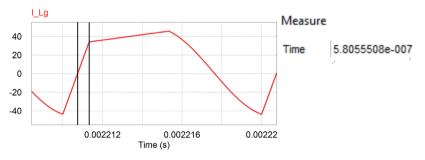
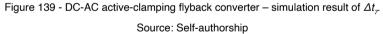


Figure 138 - DC-AC active-clamping flyback converter – simulation result of Δt_{σ} . Source: Self-authorship

Figure 139 confirms the duration of the seventh operating stage given by equation (4.40). When $\alpha = \frac{\pi}{2}$, the difference between calculations and simulation results is 0.3%.





Once the duration of the operating stages do not present any percentage variation larger than the differences of the calculated and simulated values for the currents, these are considered acceptable approximated results.

With the currents and duration of the operating stages confirmed, it is interesting to check if the ZVS really occurs for *S1* and *SG*. According to the statement in section 4.8, ZVS is achieved in both switches by delaying the PWM pulses by a minor period. In Figure 140, the simulation results show that ZVS occurs in both switches. In both Figure 140 (A) and (B), the PWM pulses were delayed for *83.33 ns*. The maximum period that the PWM can be delayed for *S1* is the duration of the sixth operating stage, in this case *745.1 ns*. However, considering that the duration of the operating stages varies with α , it is understood that ZVS may not be achieved for the whole variation of α from zero to 2π .



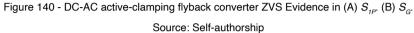
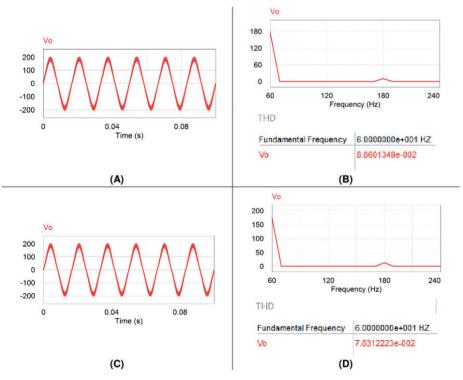
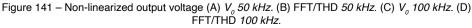


Figure 141 presents the output voltage in switching frequencies of *50 kHz* in (A) and *100 kHz* in (C). From the simulation results, it is expected that this converter present almost no low frequency harmonics, considering that the both the *50 kHz* and the *100 kHz* outputs show, respectively, only a small third harmonic in Figure 141 (B) and (D).





Source: Self-authorship

The output voltage obtained from a linearized duty cycle is presented in Figure 142. These results shows that the reduced switching frequency (50 kHz) may produce more low frequency harmonics than the original 100 kHz.

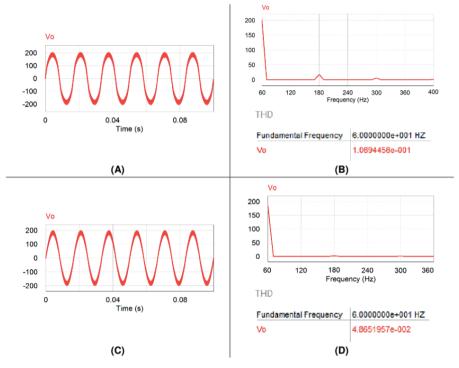


Figure 142 - Linearized output Voltage (A) V_o 50 kHz. (B) FFT/THD 50 kHz. (C) V_o 100 kHz. (D) FFT/THD 100 kHz.

Source: Self-authorship

Table 16 summarizes the most important values of the simulation. All but the identified values displayed are calculated/simulated with the same requirements presented in Table 15. Although the calculated/simulated current values are not as accurate as expected, the other differences are minimum and acceptable. An experiment was made varying the capacitor C_{g} to obtain a current waveform as close as possible to the one presented in Figure 126, which was made possible with a 10 µF capacitor. The results show that the majority of the values converge to the calculated, showing that the neglected dynamics involving the auxiliary switching capacitor can produce significant differences.

	Variable	Calculated	Simulated ²	Diff.
DMO Output Valle as	Variable			
RMS Output Voltage	VO_RMS	127 V	129.5 V	1.97 %
RMS Output Voltage (10 µF)	Vo_RMS	127 V	128.1 V	0.86 %
Peak Output Voltage	Vo	179.6 V	180.5 V	0.51 %
Output Current	Ιο (π/2)	5.568 A	5.597 A	0.53 %
Magnetizing Ind. Current IL1	IL1 (π/2)	32.381 A	32.78 A	1.24 %
Magnetizing Ind. Current IL2	IL2 (π/2)	43.81 A	44.06 A	0.58 %
Avg. Magnetizing Ind. Current	ILM	22.3 A	23.01 A	3.19 %
First Operating Stage	Δt1 (π/2)	3.954 µs	3.905 µs	1.24 %
Third Operating Stage	Δt3 (π/2)	2.343 µs	2.389 µs	1.97 %
Fourth Operating Stage	Δt4 (π/2)	2.343 µs	2.331 <i>µ</i> s	0.52 %
Sixth Operating Stage	Δt ₆ (π/2)	0.782 <i>µ</i> s	0.807 µs	3.2 %
Seventh Operating Stage	Δt7 (π/2)	0.578 µs	0.582 µs	0.7 %
Voltage on CG	VCG	-79.4 V	-75.33 V	5.13 %
Avg. Current in CG	ICG	0 A	-0.62 mA	NA
RMS Current in CG	ICG_RMS	12.447 A	14.56 A	16.98 %
RMS Current in CG (10 µF)	ICG_RMS	12.447 A	12.85 A	3.24 %
Avg. Current in S1	IS1	7.143 A	7.448 A	4.27 %
Avg. Current in S1 (10 μF)	IS1	7.143 A	7.286 A	2 %
RMS Current in S1	IS1_RMS	17.723 A	16.48 A	7.02 %
Max. Voltage on S1	VS1_max	149.401 A	158.01 V	5.77 %
Avg. Current in SP	ISP	1.772 A	1.82 A	2.71 %
RMS Current in SP	ISP_RMS	4.009 A	4.233 A	5.59 %
RMS Current in SP (10 µF)	ISP_RMS	4.009 A	4.062 A	1.32 %
Max. Voltage on DP	VDP_max	484.76 V	470 V	3.05 %

Table 16 - DC-AC active-clamping flyback converter - 100 kHz - comparative results

Source: Self-authorship

The differences between the calculated and simulated values, using the requirements of Table 15 are even more evident in Table 17, which contain the simulation results of the *50 kHz* operation. In this case, the differences are even more prominent, becoming clear that the auxiliary switching capacitor has influence on the energy transfer. However, just as previously presented in Table 16, as C_{a} is reduced, the simulated values tend to converge.

¹ All calculations available on Appendix G.

² All but the identified values were simulated with the 2 µF capacitor in CG

	Variable	Calculated ³	Simulated ⁴	Diff.
RMS Output Voltage	V0_RMS	127 V	135 V	6.3 %
RMS Output Voltage (10 µF)	Vo_RMS	127 V	124.8 V	1.76 %
Peak Output Voltage	Vo	179.6 V	178.6 V	0.56 %
Output Current	Ιο (π/2)	5.568 A	5.533 A	0.63 %
Magnetizing Ind. Current /L1	IL1 (π/2)	28.571 A	28.362 A	0.74 %
Magnetizing Ind. Current IL2	IL2 (π/2)	47.619 A	47.088 A	1.12 %
Avg. Magnetizing Ind. Current	ILM	38.095 A	37.93 A	0.44 %
First Operating Stage	Δt1 (π/2)	8.18 µs	8.1 µs	0.98 %
Third Operating Stage	Δt3 (π/2)	4.549 μs	4.65 µs	2.23 %
Fourth Operating Stage	Δt4 (π/2)	4.549 μs	4.36 µs	4.16 %
Sixth Operating Stage	Δt6 (π/2)	1.701 μs	2.02 µs	18.76 %
Sixth Operating Stage (10 µF)	Δt6 (π/2)	1.701 μs	1.6 µs	6.31 %
Seventh Operating Stage	Δt7 (π/2)	1.02 μs	1.04 µs	1.97 %
Voltage on CG	VCG	-83.869 V	-76.11 V	9.26 %
Avg. Current in CG	ICG	0 A	-0.39 mA	NA
RMS Current in CG	ICG_RMS	13.508 A	18.25 A	35.11 %
RMS Current in CG (10 µF)	ICG_RMS	13.508 A	13.98 A	3.37 %
Avg. Current in S1	IS1	7.143 A	8.081 A	13.1 %
Avg. Current in <i>S1</i> (10 μF)	IS1	7.143 A	6.907 A	3.4 %
RMS Current in S1	IS1_RMS	18.176 A	17.16 A	5.59 %
Max. Voltage on S1	VS1_max	181.127 V	174.6 V	3.61 %
Avg. Current in SP	ISP	1.772 A	1.945 A	9.77 %
Avg. Current in <i>SP</i> (10 μF)	ISP	1.772 A	1.747 A	1.43 %
RMS Current in SP	ISP_RMS	4.05 A	4.6 A	13.59 %
RMS Current in SP (10 µF)	ISP_RMS	4.05 A	3.99 A	1.5 %
Max. Voltage on DP	VDP_max	469.651 V	453.28 V	3.49 %

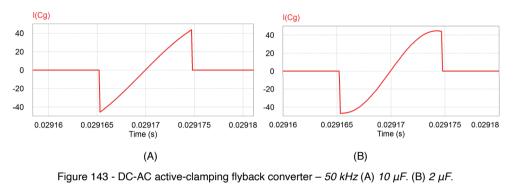
Table 17 - DC-AC active-clamping flyback converter – 50 kHz - comparative results Source: Self-authorship

The experiments varying the capacitance in $C_{_G}$ is justified by the disparity of the waveforms presented in Figure 143 (A) and (B). In (A), is presented a waveform that represents the current in the capacitor when the capacitance is 10 μ F. It is clear that, for this

³ All calculations available on Appendix H.

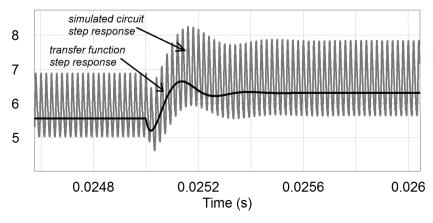
⁴ All but the identified values were simulated with the 2 µF capacitor in CG

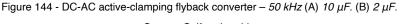
particular capacitance in this case, the waveform in (A) is similar to the theoretical waveform studied during the analysis of the converter and presented in Figure 126. However, if the capacitance is not adjusted properly, for this particular case where the dynamics of the capacitor $C_{_{G}}$ and inductor $L_{_{G}}$ and $L_{_{M}}$ are neglected, the differences between the calculated and simulated values tend to become larger as the waveform of the current approximates itself to the waveform in (B).



Source: Self-authorship

The control-to-output voltage transfer function is validated via simulation by applying a step in the duty cycle and comparing the similarity of the transient responses given by the transfer function and the simulated circuit, as presented in Figure 144. It is possible to evaluate that the simplifications made regarding the current in the magnetizing inductance presents little impact. The small error in the output voltage presented is more related to the neglected dynamic of the auxiliary and output capacitor than the current in the magnetizing inductance.





Source: Self-authorship

For this converter, a phase-locked loop (PLL) control algorithm has been developed for implementation, in case of satisfactory simulation results. The purpose of this algorithm is to adjust the phase of the output generated by the converter with the phase of the grid, which is required for grid-tied converters. Although the design of this PLL has not been studied in depth in this work, the results of this simulation is presented in Figure 145 for the converter switched at *50 kHz*, where the phase of the converter is initially dislocated 120 degrees from the grid.

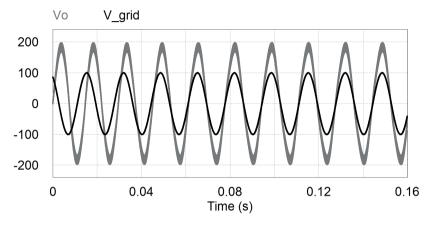


Figure 145 - DC-AC active-clamping flyback converter's linearized output voltage with PLL *50 kHz*. Source: Self-authorship

Figure 146 presents the converter switched at *100 kHz*, adjusting its phase to the grid, which is initially dislocated 120 degrees.

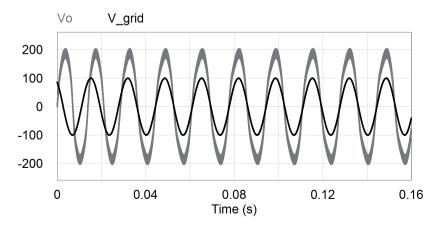


Figure 146 - DC-AC active-clamping flyback converter's linearized output voltage with PLL *100 kHz*. Source: Self-authorship

5 I CHOICE OF COMPONENTS AND PROTOTYPE BUILT

Based on the calculations and simulation results, this section highlights the main requirements adopted to choose the components for the prototype. It also presents the requirements adopted to build the flyback inductor and the winding procedure adopted.

Whereas the converter was initially intended for *100 kHz* operation, the parameters presented are loyal to its original purpose. Therefore, the *50 kHz* currents and voltages are not present in this section.

5.1 Switches and diodes

The first requirement observed to choose the switches were the maximum voltages and currents during steady-state operation. Table 18 displays the main parameters for the choice of the switches.

Because both switches *S1* and *SG* are submitted to similar values of voltages and currents, the same component is dimensioned for both switches. Similarly, due to the voltages and currents in *SP* and *SN* are identical, the component dimensioned for both is also the same.

	Variable	100 kHz ⁵
Maximum Voltage	VS1_max	149.4 V
	VSG_max	149.4 V
	VSP_max / VSN_max	359.2 V
Peak Current	IS1_max	43.81 A
	ISG_max	43.81 A
	ISP_max / ISN_max	18.41 A
Average / RMS Current	IS1 / IS1_RMS	7.143 A / 17.723 A
	ISG / ISG_RMS	0 A / 12.447 A
	ISP / ISP_RMS	1.772 A / 4.009 A

Table 18 - DC-AC active-clamping flyback converter - requirements for choice of switches. Source: Self-authorship

Based on the values of Table 18, the MOSFET chosen for this application was the

IRFP4668PBF. As the maximum voltage rated for switch is 200 V, it can only used as S_{τ} and S_{g} . An estimative of switching and conduction losses for this MOSFET is presented in

5 All calculations available on Appendix G.

Appendix I. Table 19 presents the main characteristics of this switch. In this case, the low *RDS* (on) was a factor of major importance.

	Variable	Datasheet Value
Maximum Voltage	VDSS	200 V
On Registeres	RDS (on) typ.	8 mΩ
On Resistance	RDS (on) max.	9.7 mΩ
Drain Current	ID	130 A
Maximum Power Dissipation	PD	520 W

Table 19 - MOSFET IRPF4668PBF main characteristics.

Source: Self-authorship

In the secondary windings, because of the turns ratio of the flyback inductor, the maximum voltage on the switches is higher than the voltage on the switches in the primary winding. Considering that the IGBTs used in the previous converter presented a satisfactory efficiency and overall behavior, the same switch (IKW40N65F5) was used as S_p and S_N . Table 10 displays the main characteristics of this IGBT. However, in the initial tests, the RCD clamps in the diodes and switches degraded the performance levels. In order to raise the clamped voltage, new switches were necessary. From this point onwards, the IGBT used in this application was the IHW20N120R3. Table 20 presents the main characteristics of this IGBT. The estimative of switching and conduction losses are presented in Appendix I.

	Variable	Datasheet Value
Maximum Voltage	VCE	1200 V
DC Collector Current	<i>IC</i> = 25°C	40 A
DC Collector Current	<i>IC</i> = 100°C	20 A
Pulsed Collector Current	lCpuls	60 A
Threshold Voltage	VTH	5.8 V

Table 20 - IGBT IHW20N120R3 main characteristics.

Source: Self-authorship

The process of choosing the diodes was the same as the switches. Although, for the diodes it was considered important the use of a high-frequency operation diode. Table 21

presents the main parameters used for the choice of the diodes.

	Variable	100 kHz ⁶
Maximum Voltage	VDP_max	484.76 V
Peak Current	IDP_max	18.41 A
Average / RMS Current	ISP / ISP_RMS	1.772 A / 4.009 A

Table 21 - DC-AC active-clamping flyback converter - requirements for choice of diodes. Source: Self-authorship

Based on these results, the silicon carbide schottky diode C3D06060A was chosen for this application. Table 22 presents the main characteristics of this diode.

	Variable	Datasheet Value
Repetitive Peak Reverse Voltage	VRRM	600 V
Surge Peak Reverse Voltage	VRSM	600 V
DC Blocking Voltage	VDC	600 V
Continuous Forward Current	IF (TC=25°C)	19 A
Continuous Forward Current	IF (TC=135°C)	9 A
Repetitive Peak Forward Surge Content	IFRM (TC=25°C)	30 A
nepetitive reak rotward Surge Content	IFRM (TC=135°C)	20 A
Power Dissinction	Ptot (TC=25°C)	88 W
Power Dissipation	Ptot (TC=110°C)	38 W
	VF (Tj=25°C)	Max. 1.7 V
Forward Voltage	VF (Tj=175°C)	Max. 2.4 V

Table 22 – Diode C3D06060A main characteristics.

Source: Self-authorship

5.2 Output filter capacitors

The output filter capacitors chosen for this application were generic polypropylene capacitors of 2.2 μ F / 250 V. The main reason for the choice of these capacitors were

6 All calculations available on Appendix G.

availability, ease of assembly and reliability.

5.3 Magnetics

Table 23 presents the requirements for the construction of the flyback inductors for each switching frequency. Although the converter is the same, the flyback inductors and auxiliary switching inductances need to be replaced in accordance to the switching frequency.

	Variable	100 kHz ⁷	50 kHz ⁸
AC Inductance	LM	<i>26.062</i> μH	<i>22.219 µ</i> H
Max. Current (Primary Winding)	IL2	43.81 A	47.619 A
Max. Current (Secondary Winding)	IDP_max	18.41 A	18.73 A
AC Primary Winding RMS Current	IS1_RMS	17.723 A	18.176 A
AC Secondary Winding RMS Current	IDP_RMS	4.009 A	4.05 A
Current Ripple	ΔILM	6.69 A	11.15 A
Turns Ratio	n	4.276	4.276
Switching Frequency	fs	100 kHz	50 kHz

Table 23 - DC-AC active-clamping flyback converter – requirements of the flyback inductors. Source: Self-authorship

In order to decrease the leakage inductance of the flyback inductor, it was used in these inductors the litz wire, which is intended to reduce the skin and proximity effects. The whole design of the *100 kHz* inductor is presented in Appendix J and the *50 kHz* in Appendix K.

The winding technique adopted is the same as presented in Figure 61. However, because these coupled inductors have two separate secondary windings, the resultant cross-section of these inductors is more similar to the drawing presented in Figure 147, where half of each winding is wound in sequence.

⁷ Design presented in Appendix J.

⁸ Design presented in Appendix K.

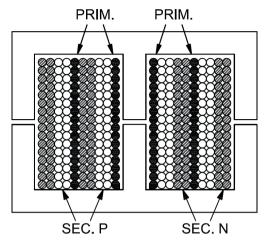


Figure 147 – DC-AC active-clamping flyback converter – inductor winding technique. Source: Self-authorship

The requirements for the construction of the auxiliary switching inductor are presented in Table 24.

	Variable	100 kHz [°]	50 kHz ¹⁰
AC Inductance	LG	2 µH	4 µH
Max. Current	IL2	43.81 A	47.619 A
Min. Current	-1L2	- 43.81 A	- 47.619 A
RMS Current	ILG_RMS	20.452 A	21.497 A
Current Ripple	ΔILG	85.62 A	95.238 A
Max. Voltage	VLG_max	112 V	112 V

Table 24 - DC-AC active-clamping flyback converter – requirements of the auxiliary inductors. Source: Self-authorship

The design of the *100 kHz* inductor is presented in Appendix L and the *50 kHz* is presented in Appendix M. Both these auxiliary inductors were wound with litz wire.

5.4 Auxiliary switching capacitor

The parameters used to choose the auxiliary switching capacitance are presented in Table 25.

⁹ Design presented in Appendix L.

¹⁰ Design presented in Appendix M.

	Variable	100 kHz
Capacitance	CG	2 µF
Max. Current	IL2	43.81 A
Min. Current	-1 <u>L2</u>	- 43.81 A
RMS Current	ICG_RMS	12.447 A
Max. Voltage	VCG_max	149.4 V

Table 25 - DC-AC active-clamping flyback converter – requirements of the auxiliary switching capacitor. Source: Self-authorship

The capacitor chose was the generic polypropylene $4\mu7 F / 250 V$. The PCB was designed to use two capacitors in parallel to ease any modification, if necessary. Therefore, the equivalent capacitance utilized was of $2\mu3 F$.

5.5 Clamp circuit

To reduce the effects of hard-switching in the secondary windings of the flyback inductors, it is employed a single RCD clamp circuit to clamp the voltage over the diode and the switch. This circuit is presented in Figure 148. Considering that the maximum voltages and currents are the same for D_p/D_N and S_p/S_N , the circuit is also the same.

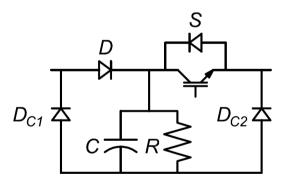


Figure 148 – DC-AC active-clamping flyback converter – RCD clamp circuit. Source: Self-authorship

Similar to the converter presented in Chapter 3 the RCD clamp resistance was adjusted throughout the initial tests. Better efficiency levels were observed using two 5W 56 k Ω in series, which is coincidentally the same equivalent resistance of the clamp circuit adjusted for the converter presented in Chapter 3. The same capacitor of 1 μ F /400 V was used as well. On the other hand, the diodes did not have to support as much current as

the MUR460 of the other circuit. In this case, the diodes used were the MUR1100, whose average rectified current is 1 A, the maximum instantaneous forward voltage is 1.75V @ 25o C and the maximum dc blocking voltage is 1000 V.

5.6 Prototype

Figure 149 presents a picture of the prototype built under the specifications presented in the previous sections of this chapter.

The test setup comprises the following equipment:

- Texas Instruments TMS320F28335 DSP: Used to generate the command pulses and AD converter;
- Tektronix DPO754C oscilloscope: all waveforms presented.
- Yokogawa WT500 power meter: efficiency measurements.



Figure 149 - DC-AC active-clamping flyback converter – prototype. Source: Self-authorship

6 | EXPERIMENTAL RESULTS

This section presents the experimental results of the converter operating in two different switching frequencies. Different capacitors were used between the drain and source of the switches *S1* and *SG*, leading to different efficiency levels, which are further added at the efficiency tests section.

The results presented in this section show the converter operating only with the PLL algorithm because the difference in terms of efficiency with or without the algorithm was minimal.

6.1 100 kHz – Linearized output

The output voltage of the converter presented visible harmonic distortion operating with a switching frequency of *100 kHz* as presented in Figure 150. Throughout the experiments, it has been proven that this harmonic distortion is not primarily a product of the converter trying to follow a distorted grid voltage as reference, even though it has its contribution. The value of the output voltage in Figure 150 is the rated *127VRMS* of the converter.

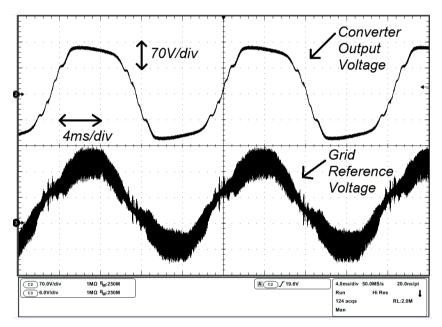


Figure 150 - DC-AC active-clamping flyback converter - PLL output voltage Source: Self-authorship

As expected, output voltage and current are in phase, as Figure 151 presents. In this acquisition, the RMS value of the voltage is *127V* and the RMS current is *4.1 A*.

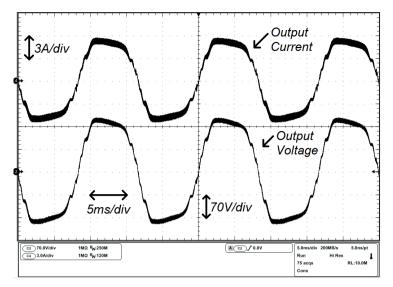
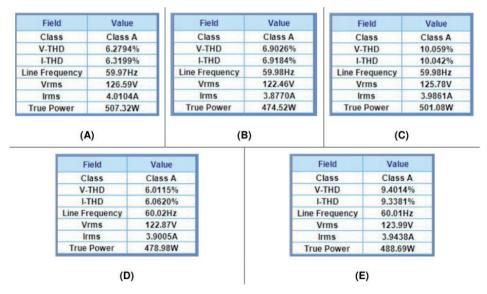
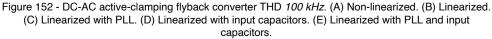


Figure 151 - DC-AC active-clamping flyback converter - *100 kHz* output current and voltage. Source: Self-authorship

The converter is then submitted to several analyses of total harmonic distortion, which results are presented in Figure 152.





Source: Self-authorship

In Figure 152 (A), is presented the THD analysis for the converter operating without its linearization. As expected from the comparison of Figure 141 and Figure 142, the THD is higher with the converter operating with the linearized function, as (B) shows, although the efficiency increases. Another factor that can take the harmonic distortion to even higher levels is the PLL algorithm, as Figure 152 (C) shows. A speculative test was made with a capacitor bank composed of four capacitors of $470 \,\mu\text{F}$ in parallel connected in parallel with the input of the converter to filter a possible voltage distortion caused by the high-frequency switched power supply. The results were significantly improved with the linearization of the duty cycle (Figure 152 (D)) and presented notable reduction in the current and voltage distortion once linearized and operating with the same PLL algorithm.

The ZVS operation of the converter in both switches were then verified. Figure 153 presents the gate-to-source voltage (*VGS*) and the equivalent drain-to-source voltage (*VDS*) in S_1 when the output voltage is maximum at $\alpha = \frac{n}{2}$. The maximum voltage on S_1 in this acquisition is 193 V.

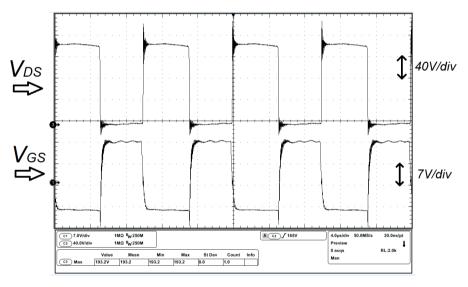


Figure 153 - DC-AC active-clamping flyback converter - 100 kHz switch S_{i} . Source: Self-authorship

Figure 154 shows that, when the output voltage is at 164 V, ZVS is achieved in S1. The deadtime in this acquisition is 300 ns, but experiments were performed varying it from 90 ns to 1 μ s and ZVS was still achieved when the output voltage is at its peak in rated output power.

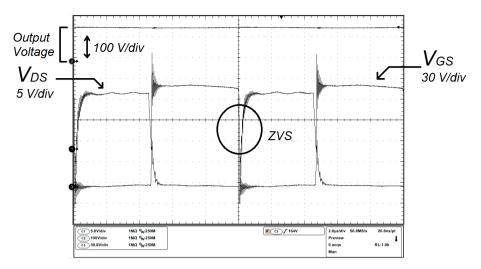


Figure 154 - DC-AC active-clamping flyback converter - 100 kHz S_1 ZVS for V_0 =164 V. Source: Self-authorship

However, as the output voltage decreases and the deadtime is maintained the same from $\alpha = 0$ to $\alpha = 2\pi$, the switching becomes dissipative. Overall, for rated output power, from 0 V to 40 V or -40 V, the switching is dissipative for a switching frequency of 100 kHz and deadtime of 300 ns. Figure 155 presents the dissipative switching of S1.

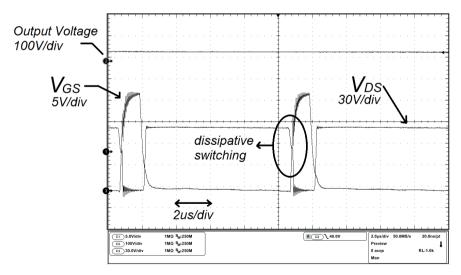


Figure 155 - DC-AC active-clamping flyback converter - 100 kHz S_1 dissipative switching for V_0 =40 V. Source: Self-authorship

Figure 156 presents the gate-to-source voltage (V_{GS}) and equivalent drain-to- source voltage (V_{DS}) in S_{G} , when the output voltage is maximum at $\alpha = \frac{\pi}{2}$. The maximum voltage

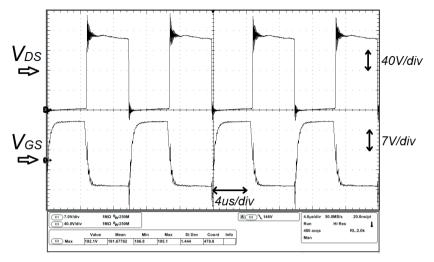


Figure 156 - DC-AC active-clamping flyback converter - 100 kHz switch S_{g} . Source: Self-authorship

As the PWM pulses of $S_{_G}$ are complementary to $S_{_{7}}$, the deadtime in $S_{_G}$ is the same of $S_{_{7}}$. Figure 157 presents the soft switching of $S_{_G}$ when the output voltage is close to its maximum.

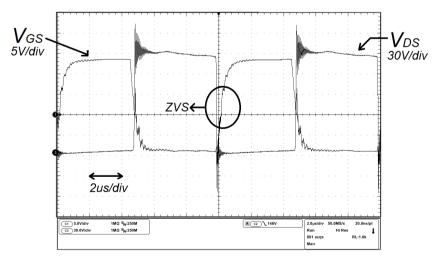


Figure 157 - DC-AC active-clamping flyback converter - 100 kHz S_{g} ZVS for V_{o} =164 V. Source: Self-authorship

It is interesting to notice that, under the same circumstances that caused S1 to lose

soft switching, S_{G} remains in ZVS. Figure 158 shows the voltage on S_{G} and its command pulse when the output voltage is at -6 V.

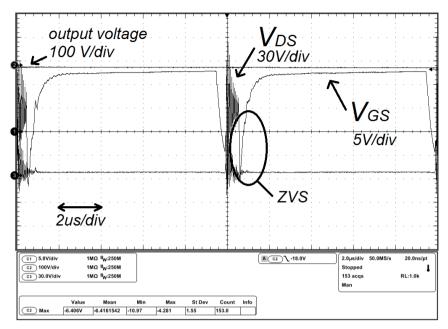


Figure 158 - DC-AC active-clamping flyback converter - 100 kHz $S_{_G}$ ZVS for $V_{_0}$ =-6 V. Source: Self-authorship

In the secondary winding of the flyback inductor, the voltage on the diodes D_p and D_N switches S_p and S_N is clamped around 400 V. As commented in section 5.5.1, the switches had to be resized to cope with the higher voltage when the output voltage is maximum. In Figure 159, the voltage on S_p is presented, as well as its gate-to- source voltage and how the clamp voltage behaves as the output voltage alternates.

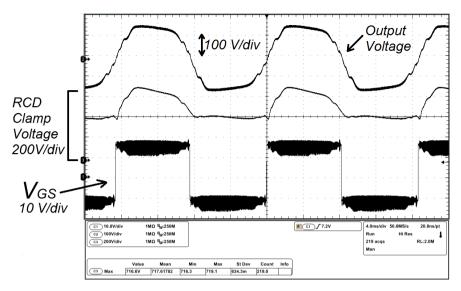


Figure 159 - DC-AC active-clamping flyback converter - 100 kHz S_p clamp voltage. Source: Self-authorship

6.2 50 Khz - Linearized output

Once, the results of the converter operating at a switching frequency of *100 kHz* did not present the results expected in terms of efficiency and harmonic distortion, the possibility of replacing the auxiliary switching inductor and flyback inductor was considered. The results presented for the 100 kHz operation were already acquired from the second prototype built, where significant improvements on the efficiency were observed, although the same was not observed in the output waveforms. It is worth mentioning that the intent of replacing the magnetics was to turn possible the verification of any effect caused by parasitic inductances, which could be one of the causes of the distorted output waveforms. Considering that the waveform distortion has been observed in both converters built and that the same magnetics were used for testing, it was worth checking a possible variation of the issue, as well as inquiring on the effects caused by the switching frequency.

The result of the output current and voltage in phase with the grid reference voltage, operating in the switching frequency of 50 kHz, is presented in Figure 160 for rated output power. It is noticeable that, even though the harmonic distortion is still present in the output of the converter, the 50 kHz switching frequency presented reduced lower frequency harmonics, in this case.

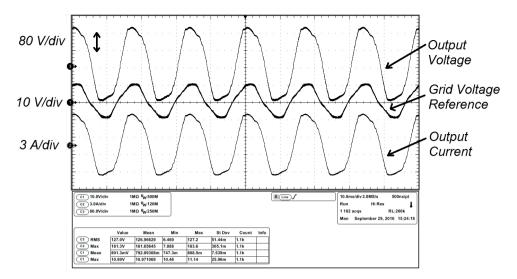


Figure 160 - DC-AC active-clamping flyback converter - *50 kHz* PLL output current and voltage. Source: Self-authorship

To draw a comparison with the tests made with the operation at *100 kHz*, the converter was then submitted to several THD tests, which results are presented in Figure 161.

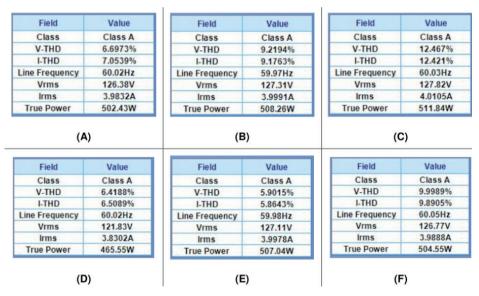


Figure 161 - DC-AC active-clamping flyback converter THD 50 kHz. (A) Non-linearized. (B) Linearized. (C) Linearized with PLL. (D) Non-linearized with input capacitors. (E) Linearized with input capacitors. (F) Linearized with PLL and input capacitors.

Source: Self-authorship

In Figure 161 (A), the THD of the converter is presented for a non-linearized duty cycle operation; whereas in (B) it is possible to verify that, in this case, the linearization has added some harmonic distortion, as the results increased *2.51* %. As expected, in (C) the PLL adds even more distortion, as for this situation the converter has to not only follow a sinusoidal reference, deforming the duty cycle as a function of the voltage conversion ratio, but also to keep the generated output in the phase with the grid. Considering that the improvements observed were not as significant as expected from the *100 kHz* operation, the same tests were performed with the input capacitors. As a result, the THD of the previous three experiments performed were improved; as presented in Figure 161 (D) for the non-linearized operation with the input capacitor; in (E) for the linearized with input capacitor; and finally in (D) for the linearized duty cycle operating with PLL and the input capacitors.

Figure 162 shows the waveforms of the input and output voltages that presented the best THD result, namely the test performed with the input capacitors with the converter operating with linearized duty cycle.

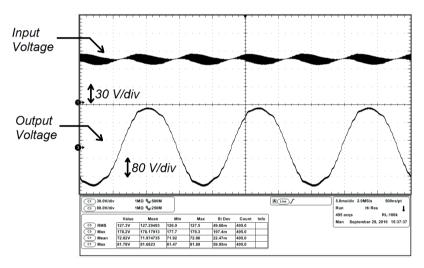


Figure 162 - DC-AC active-clamping flyback converter – input and output voltage – 50 kHz linearized with input capacitor.

Source: Self-authorship

The drain-to-source voltage (VDS) and gate-to-source voltage (VGS) on the main switch *S1*, for rated output power is presented in Figure 163. For the *50 kHz* switching frequency, the deadtime of the converter was reduced to *200 ns*, as better efficiency result were observed.

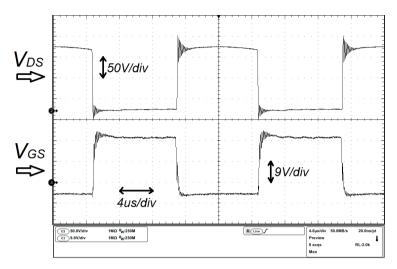


Figure 163 - DC-AC active-clamping flyback converter - 50 kHz Switch $S_{\tau} V_{GS}$ and V_{DS} . Source: Self-authorship

In Figure 164, ZVS is presented in switch *S1* when $\alpha = \mathcal{V}_2$. The maximum voltage on S_1 did not change with the switching frequency modified, which means that for rated output power the maximum voltage on S_1 is 193 V.

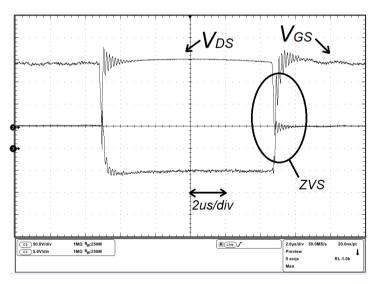


Figure 164 - DC-AC active-clamping flyback converter - 50 kHz ZVS on switch S_{γ} . Source: Self-authorship

The drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltages on S_{G} are presented in Figure 165 for rated output power. The maximum voltage, just as in S_{η} , remains the same

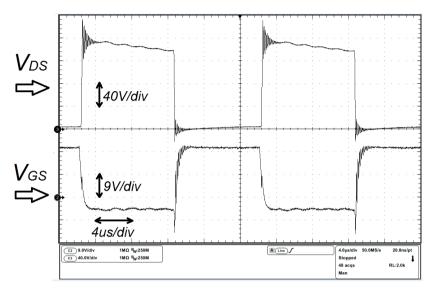


Figure 165 - DC-AC active-clamping flyback converter - 50 kHz switch $S_{_G} V_{_{GS}}$ and $V_{_{DS}}$. Source: Self-authorship

ZVS is achieved in S_{G} for rated output power, as presented in Figure 166.

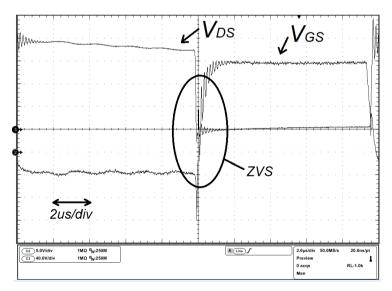


Figure 166 - DC-AC active-clamping flyback converter - 50 kHz switch $S_{G} V_{GS}$ and V_{DS} . Source: Self-authorship

In Figure 170, is possible to identify the variation of the output current corresponding to the complementary switching of S_{ρ} and S_{N} .

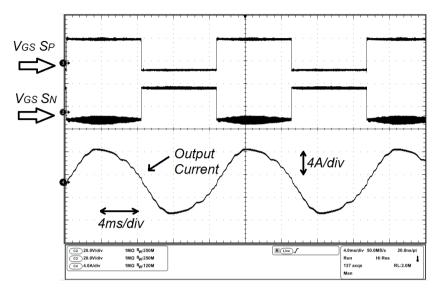
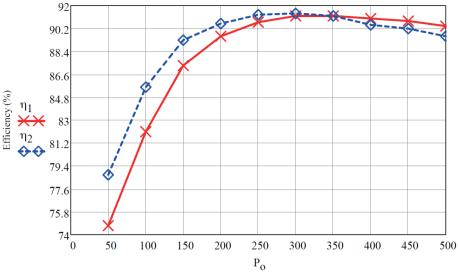


Figure 167 - DC-AC active-clamping flyback converter - 50 kHz switch S_p and S_N . Source: Self-authorship

6.3 Efficiency tests

As the tests progressed, efficiency tests were performed indicating that better results are obtained with an additional capacitor connected in parallel with switches *S1* and *SG*. The capacitance used for these tests were 1 *nF*, 5.6 *nF* and 10 *nF* and with no capacitor at all. Within the power range that the converter was originally designed, the results of the operation with the capacitor of 10 *nF* did not present any improvement from the 1 *nF* and 5.6 *nF* capacitors for both switching frequencies. It is interesting to notice that without any parallel capacitance, the efficiency of the converter does not present any sign of improvement as well. Figure 168 presents the results of the converter operating with switching frequency of 100 *kHz*, where η 1 presents the efficiency curve with a parallel capacitor of 5.6 *nF* and η 2 with a 1 *nF* capacitor.

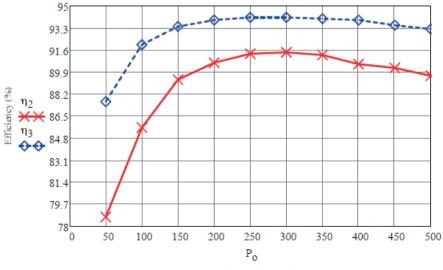
It is noteworthy that, for the converter designed, depending on the power range in which the converter will operate longer, different capacitors can provide better overall efficiency. However, regardless of the capacitor used in parallel with S_1 and S_G , the converter reaches its maximum efficiency operating at 300 W. For rated output power, the best efficiency result achieved was 90.4% with the 5.6 nF capacitor in parallel with S_1 and S_G .



Active Output Power (W)

Figure 168 - DC-AC active-clamping flyback converter - *100 kHz* efficiency results (η 1=5.6 nF / η 2=1 nF). Source: Self-authorship

Figure 169 presents a comparison of the efficiency curve obtained using the *1.6 nF* capacitor with the calculated efficiency curve, calculated as presented in Appendix I. Based on this comparison, new inductors were designed for operation at *50 kHz*, as previously explained.



Active Output Power (W)

Figure 169 - DC-AC active-clamping flyback converter - 100 kHz efficiency results (η 2=5.6 nF / η 3=calculated efficiency).

Source: Self-authorship

Once the flyback inductor and the auxiliary switching inductor were replaced, the same efficiency tests were performed with the same capacitors in parallel with S_{τ} and S_{G} . Figure 170 shows the efficiency results of the converter operating a switching frequency of *50 kHz*.

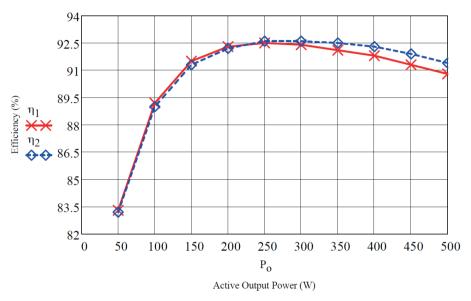
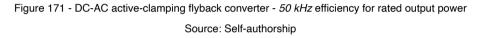


Figure 170 - DC-AC active-clamping flyback converter - 50 kHz efficiency results (η 1=5.6 nF / η 2=1 nF). Source: Self-authorship

The improvements in the results from the *100 kHz* to *50 kHz* are considerable. For every point of the curve, the *50 kHz* operation presented better results, due to the reduction of the switching losses. However, for this operation, the best results were obtained for an output power of 250 W, where the curve reached the highest point of 92.6%. For rated output power, the best result achieved was 91.48%, as Figure 171 depicts. All tests were performed with resistive loads.

Normal Mode	Uover:=== Scaling:= LineFilt: lover:=== Average:= FreqFilt:	NULL:= YOKOGAWA 🔶 CF:3
😫 + ISET : change it	iems	PAGEElement1
Udc1	70.20 v	
Idc1	8.144 _A	2 Element2 U2 600V 12 10A
P1	0.5640 kw	3 Element3 4 U3 60V
Urms	2 127.15 v	5 13 10Å
Irms	2 4.059 🗚	6 7
P2	0.5160 kw	8
71	91.482 🗴	Integ:Reset_
		Time
Update 9031(1se	c)	2016/07/04 14:12:16



7 | CONCLUSION

This chapter presented the validation of the mathematical models studied in Chapter 4 by means of numeric simulation and experimentation. The simulation results show that the simplifications made while modeling the converter, offer a good starting point for choice of components and prototyping. Although the energy transfer involving the capacitor C_{g} to the output of the converter was neglected during the modeling, the experimental results did not present any implications that could invalidate the analyses or the prototype.

Initially, the idea of this converter was to evidence that soft switching techniques can reduce the issue caused by the voltage surges in the primary windings of the flyback inductor and, as a result, the converter would reach higher efficiency levels, all of whom were observed in the experimental results shown. As presented in Figure 171 the higher efficiency level obtained for rated output power was *91.42* %. It is also interesting to see that better efficiency levels and total harmonic distortion were obtained in the converter operating with switching frequency of *50 kHz*. It is understood that the efficiency has improved as much as observed, due to the reduction of the switching losses by means of the change in the switching frequency (from 100 kHz to 50 kHz). In this case, the change of magnetics offered little or no influence, as the winding procedure and wire used were the same, and the values of both magnetizing and leakage inductances were very similar.

Still, some improvements can be considered in the future for this prototype, such as the substitution of the IGBT switches used as S_{ρ} and S_{N} , which would require an adjustment on the resistor of the RCD clamp, presented on the circuit of Figure 148. As the IGBT

switches used in this prototype are suited for 1200 V applications and the maximum voltage registered was of 716 V (Figure 157), it is possible that other switches could improve the overall efficiency.

The clamp circuit was designed to accommodate both switch and diode in the same circuit. This decision was made based on preliminary tests performed with the first prototype assembled for this application, where the initial intent was to clamp only the voltage on the switch. As the results were not considered satisfactory, due to the switching losses in the RCD clamp of S_{ρ} and $S_{N^{\prime}}$ the circuit presented on Figure 148 was designed and included in the second prototype built, which results are presented throughout this chapter and present a big improvement on the previous experience.

As for THD, further investigation is needed in regard to the root cause of the problem. Initial studies were performed changing the switching frequency from 100 kHz to 50 kHz and replacing the magnetic components (LG and LM). Once the results did not show any particular improvement related, other areas need to be carefully analyzed. As the power supply clearly adds a 120 Hz component to the converter, the input capacitor bank tend to minimize this effect as the THD results presented in this chapter. However, it was expected from this converter to operate below the 4 % THD margin and, in that aspect, one control related area was not explored hereon. The form of generating the linearized duty cycle to operate the PWM in this work required the DSP to calculate the duty cycle for every switching period. This calculation can be excluded by creating a lookup table that corresponds the variation of the reference to its equivalent duty cycle value. The benefits of this operation were not explored in this piece of work.

Despite the superior efficiency, this converter operating in these two switching frequencies is not well suited for open-loop offline applications, due to the high harmonic distortion it presents at its output. On the other hand, once connected to the utility grid in a closed-loop configuration, this distortion tend to disappear, as the grid itself imposes the voltage.

GENERAL CONCLUSION

The dc-ac converters studied hereon present an interesting solution for a singlestage application. The first is a single-stage high-frequency-isolated converter that offers an option for offline applications, considering that it presented reduced total harmonic distortion combined with good power efficiency. The second is also a single- stage converter that makes use of the flyback inductor to provide galvanic isolation. In this second converter, the efficiency levels are a standout characteristic.

For the dc-ac flyback converter with differential output connection, the main contributions of this work are the additional switching strategy studied and the new studies that provide the transfer functions for both switching strategies of the converter coupled to an output voltage source. Although the bidirectional possibility was not explored, the converter was tested for a nonlinear load. As for the dc-ac active- clamping flyback converter the main contribution is a complete study of a new topology of the flyback inverter that employs an active-clamp circuit, improving the efficiency by means of soft-switching techniques.

In the study of the dc-ac flyback converter with differential output connection, it is shown that the new switching strategy proposed offers improved efficiency over the traditional complementary switching strategy for both linear and nonlinear loads. However, the overvoltage caused by the leakage inductance is a limiting factor to the potential of the converter. As suggestions for the sequence of the studies are the connection with the utility grid and validation of the transfer function presented in sections 2.2.10 and 2.3.10. In addition, an active-clamping circuit for the switches in the primary winding combined with different winding techniques and/or utilization of the litz wire in the flyback inductors will more than likely improve the efficiency of the converter.

It was verified that the overvoltage issue in the primary winding of the flyback inductor was minimized in the converter that operates with the active-clamp circuit in the dcac active-clamping flyback converter. This circuit, combined with the better use of the turns ratio of the flyback inductor allowed the converter to increase the efficiency levels. However, for an offline application, more time needs to be invested to verify whether the harmonic distortion is caused by the topology itself, the switching frequency or if it was a constructive issue of the prototype presented. It is worth mentioning that another PCB were designed and tested before the *50 kHz* experiment.

The results were improved in terms of efficiency but not as much in terms of harmonic distortion. As a suggestion for future studies with this converter is the connection of the to the utility grid. In addition, the clamping voltage in the secondary winding of the flyback inductor can be reduced and better semiconductor technologies can be applied in order to reduce the conduction losses. It is also interesting to ascertain if the duty cycle previously determined by a look up table offers a benefit in reducing the total harmonic distortion of the converter.

Lastly, the author would like to say that this work gave fundamental and precious knowledge in power electronics and that this journey allowed enormous professional and personal growth.

REFERENCES

ABRAMOVITZ, A. et al. Isolated Flyback Half-Bridge OCC Micro-Inverter. **IEEE Energy Conversion Congress and Exposition (ECCE)**, 14-18 September 2014. 2967-2971.

ABRAMOVITZ, A.; CHIH-SEHNG, L.; SMEDLEY, K. State-Plane Analysis of Regenerative Snubber for Flyback Converters. **IEEE Transactions on Power Electronics**, v. 28, n. 11, p. 5323-5332, 2013.

ANEEL. BIG - Banco de Informações de Geração, 2016. Disponivel em: http://www2.aneel.gov.br/ aplicacoes/capacidadebrasil/capacidadebrasil.cfm>. Acesso em: 15 jul. 2016.

BRASIL, A. Agencia Brasil - Pesquisa e Inovação, 06 mar. 2016. Disponivel em: http://agenciabrasil.ebc.com.br/pesquisa-e-inovacao/noticia/2016-03/em-oito-anos-mais-de-1-milhao-de-brasileiros-devem-gerar-sua. Acesso em: 15 jul. 2016.

CACERES, R. O.; BARBI, I. A boost DC-AC converter: analysis, design, and experimentation. **IEEE Transactions on Power Electronics**, v. 14, n. 1, p. 134-141, 1999.

CALZO, G. L. et al. LC Filter Design for On-Grid and Off-Grid. **Energy Conversion Congress and Exposition (ECCE), 2013 IEEE**, 15-19 Sept. 2013.

CAO, W. et al. Two-stage PV inverter system emulator in converter based power grid emulation system. **2013 IEEE Energy Conversion Congress and Exposition**, 15- 19 September 2013. 4518 - 4525.

CARDOSO, R. L. **Conversores CC-CAs Bidirecionais Isolados em Alta Frequencia**. 230 [f.]. Tese (Doutorado em Engenharia Elétrica) - UFSC. Florianópolis: [s.n.], 2007.

CHEN, L. et al. Design and Implementation of Three-Phase Two-Stage Grid- Connected Module Integrated Converter. **IEEE Transactions on Power Electronics**, v. 28, n. 8, p. 3881 - 3892, 2013.

CIASOLAR. Disponivel em: http://ciasolarenergia.com.br/aneel-apresenta-o- crescimento-aceleradoda-geracao-distribuida-em-2015/>. Acesso em: 15 jul. 2016.

CIMADOR, G.; PRESTIFILIPPO, P. An Attractive New Converter Topology for AC/DC, DC/DC & DC/ AC Power Conversion. Proc. of INTELEC'90. [S.I.]: IEEE. 1990. p. 597-604.

ERICKSON, R. W. Fundamentals of power electronics. [S.I.]: Chapman and Hall, 1997.

HAIBING, H. A Single-Stage Microinverter Without Using. **IEEE Transactions on Power Electronics**, v. 28, n. 6, p. 2677-2687, 2012.

HARADA, K.; SAKAMOTO, H.; SHOYAMA, M. **Phase-controlled dc-ac converter with high-frequency switching**. Trans. Power Electron. [S.I.]: [S.I.] IEEE. 1988. p. 177-180.

HU, B.; CHANG, L.; XUE, Y. Research on a novel buck-boost converter for wind turbine systems. **2008** IEEE International Conference on Sustainable Energy Technologies, 24-27 Nov. 2008. 228 - 233. IEA. Measuring the value of next-generation wind and solar power, 02 jun. 2016. Disponivel em: http://www.iea.org/newsroomandevents/news/2016/june/measuring-the-value-of-next-generation-wind-and-solar-power.html). Accesso em: 21 jul. 2016.

IEA STATISTICS. Electricity Information 2015, 2016. Disponivel em: <a href="http://www.iea.org/publications/freepublications/publicatio

IIDA, T.; BHAT, A. K. S. Zero-Voltage Transition Flyback Inverter for Small Scale Photovoltaic Power System. **36th Power Electronics Specialists Conference**, 16 June 2005. 2098-2103.

J., B.; A., J. Single phase DC/AC bi-directional converter with high frequency isolation. **RIEE&C**, **REVISTA DE INGENIERÍA ELÉCTRICA**, **ELECTRÓNICA Y COMPUTACIÓN**, **VOL. 2 NO. 1**, 2006.

JAIN, C.; SINGH, B. A single-phase two-stage grid interfaced SPV system with adjustable DC link voltage for VSC under non ideal grid conditions. **Power Electronics, Drives and Energy Systems** (PEDES), 2014 IEEE International Conference on, 16-19 December 2014. 1-6.

JOHNY, L. M. K.; SHAFEEQUE, K. M. PV fed Flyback DC-AC Inverter with MPPT Control. International Conference on Magnetics, Machines & Drives, 2014.

KASA, N.; IIDA, T.; BHAT, A. K. S. Zero-Voltage Transition Flyback Inverter for Small Scale Photovoltaic Power System. **IEEE 36th Power Electronics Specialists Conference**, 16 June 2005. 2098-2103.

KASA, N.; IIDA, T.; CHEN, L. Flyback Inverter Controlled by Sensorless Current MPPT for Photovoltaic Power System. **IEEE Transactions on Industrial Electronics**, v. 52, n. 4, p. 1145-1152, 2005.

KIM, Y. et al. A new control strategy of active clamped flyback inverter for a photovoltaic AC module system. **Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on**, 30 - 03 May - June 2011. 1880-1885.

LI, X. et al. Coordinated Control Research of Grid-Connected Two-Stage Power Converter System. **2012 Asia-Pacific Power and Energy Engineering Conference**, 27-29 March 2012. 1-5.

MARIKKANNAN, A.; MANIKANDAN, B. V.; JAYANTHI, S. A digital current controlled soft-switching DC-DC converter with high voltage gain for renewable energy sources. **Circuit, Power and Computing Technologies (ICCPCT), 2014 International Conference on**, 20-21 March 2014. 594-600.

MAROUANI, R.; ECHAIEB, K.; MAMI, A. Sliding mode controller for buck-boost dc- dc converter in PV grid-connected system. **2012 16th IEEE Mediterranean Electrotechnical Conference**, 25-28 March 2012. 281-284.

MAZUMDER, K. S.; S., M. A Low-Device-Count Single-Stage Direct-Power-. Power Electronics for Distributed Generation Systems (PEDG), 2012 3rd IEEE International Symposium on. Aalborg: IEEE. 1012. p. 725-730.

MENESES, D. et al. **Single-Stage Grid-Connected Forward Microinverter with Constant Off-Time Boundary Mode Control**. Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE. Orlando, FL: IEEE. 2012. p. 568-574.

MO, Q. et al. Research on a non-complementary active clamp flyback converter with unfolding DC-AC inverter for decentralized grid-connected PV systems. **IEEE Energy Conversion Congress and Exposition**, 17-22 September 2011. 2481-2487.

MUKHERJEE, A.; PAHLEVANINEZHAD, M.; MOSCHOPOULOS, G. A Novel ZVS

Resonant-Type Flyback Microinverter with Regenerative Snubber. **IEEE Applied Power Electronics Conference and Exposition - APEC**, 16-20 March 2014. 2958 - 2964.

RAMLI, M. Z. **A Bidirectional Inverter with High Frequency**. Power Engineering Conference, 2003. PECon 2003. Proceedings. National. Johor Bahru, Malaysia: IEEE. 2003. p. 71-75.

RIBEIRO, H.; PINTO, A.; BORGES, B. Single-Stage DC-AC Converter for Photovoltaic Systems. **2010 IEEE Energy Conversion Congress and Exposition**, 12-16 September 2010. 604-610.

SALAM, Z. et al. An Isolated Bidirectional Inverter Using High Frequency Center-Tapped Transformer. Power Electronics, Machines and Drives, 2004.

(PEMD 2004). Second International Conference on (Conf. Publ. No. 498). Edinburgh, UK: [s.n.]. 2004.

SARANYA, P. S.; CHANDRAN, L. R. Analysis of Bidirectional Flyback Converter. **Computation of Power, Energy Information and Communication (ICCPEIC), 2015 International Conference on**, 22-23 April 2015. 425-429.

SHIMIZU, T.; WADA, K.; NAKAMURA, N. Flyback-Type Single-Phase Utility Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System. **IEEE Transactions on Power Electronics**, v. 21, n. 5, p. 1264-1272, 2006.

SKINNER, A. J. **Bidirectional Continuous-mode Flyback Inverter**. Power Electronics and Applications, 1993., Fifth European Conference on. Brighton: [s.n.]. 1993.

SUKESH, N.; PAHLEVANINEZHAD, M.; PRAVEEN, J. Novel Scheme for Zero Voltage Switching of Single Stage Photovoltaic Micro-Inverter. **Applied Power Electronics Conference and Exposition** (APEC), 2013 Twenty-Eighth Annual IEEE, 17-21 March 2013. 60 - 67.

SYAM, M. S.; KAILAS, T. S. Grid connected PV system using Cuk converter. **Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), 2013 Annual International Conference on**, 4-6 June 2013. 1-6.

THANG, T. V. et al. **Analysis and Design of a Single-Phase Flyback Microinverter on CCM Operation**. 7th International Power Electronics and Motion Control Conference - ECCE Asia. Harbin, China: IEEE. 2012. p. 1229-1234.

VARTAK, C.; ABRAMOVITZ, A.; SMEDLEY, K. M. Analysis and Design of Energy Regenerative Snubber for Transformer Isolated Converters. **IEEE Transactions on Power Electronics**, v. 29, n. 11, p. 6030-6040, 2014.

APPENDIX A

APPENDIX A – CALCULATIONS FOR THE DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUTPUT CONNECTION – COMPLEMENTARY SWITCHING STRATEGY

DC-AC Flyback Converter with Differential Output Connection Complementary Switching Strategy

1. Design Specifications:

Input Voltage:	V _{IN} := 70V
RMS Output Voltage:	$V_{ef} \coloneqq 127V$
Output Power:	P ₀ := 500W
Switching Frequency:	$f_s \approx 20 kHz$
Grid Frequency:	$f_r := 60Hz$
Current Ripple Lm:	$\Delta I_{L\%} := 50\%$
Output Voltage Ripple:	$\Delta V_{\%} \simeq 0.5\%$
AC Output Voltage Ripple:	$\Delta V_{\%_{AC}} = 29\%$
Flyback Inductor Turns Ratio:	n := 1
Duty Cycle (0VAC):	D ⊨ 0.5
Switching Period:	$T_s := \frac{1}{f_s}$

2. Preliminary Calculations:

Peak Voltage:

 $V_0 := V_{eff} \sqrt{2}$ $V_0 = 179.605 V$

Modulation Index:

N

$$I := \frac{V_0}{V_{IN'}n} \qquad M = 2.566$$

2.1 DC Preliminary Calculations:

DC Output Current:

$$\begin{split} I_{o} &:= \frac{P_{o}}{V_{o}} & I_{o} = 2.784 \text{A} \end{split}$$
 DC Load Resistance:
$$R_{o} &:= \frac{V_{o}}{I_{o}} & R_{o} = 64.516 \,\Omega \end{split}$$

DC Input Current:

 $I_{IN} := \frac{P_0}{V_{IN}}$

 $T_s = 50 \ \mu s$

DC Current Ripple:

 $\Delta I_L := I_0 \cdot \Delta I_{L\%}$

$$\Delta I_{L} = 1.392 \text{ A}$$

2.2 A C Preliminary Calculations:

Max AC Output Current:

$$I_{o_AC} := \frac{2 \cdot P_o}{V_o}$$

 $I_{0_{AC}} = 5.568 A$

AC Load Resistance:

$$R_{o_AC} := \frac{V_o}{I_{o_AC}} \qquad \qquad R_{o_AC} = 32.258\,\Omega$$

AC Input Current:

$$I_{IN_AC} := \frac{2 \cdot P_o}{V_{IN}} \qquad I_{IN_AC} = 14.286 \text{ A}$$

Max AC Output Current Ripple:

$$\Delta I_{L_AC} \coloneqq I_{0_AC} \cdot \frac{\Delta I_{L\%}}{2} \qquad \Delta I_{L_AC} = 1.392 \text{ A}$$

AC Output Current:

 $I_{AC}(\alpha) := I_0 AC \sin(\alpha)$

3 - Output Characteristics 3.1 - DC Output

Duty Cycle - DC:

$$D_{max} := \frac{M - 2 + \sqrt{M^2 + 4}}{2 \cdot M}$$
 $D_{max} = 0.744$

S1P (D) - tON:

$$T_{maxP} := \frac{D_{max}}{f_s}$$

T_{max}p = 37.211 μs

V_{peak} = 179.605 V

 $V_a = 203.664 V$

S1N (1-D) - tOFF:

$$T_{maxN} := \frac{1 - D_{max}}{f_s} \qquad T_{maxN} = 12.789 \cdot \mu s$$

Max Output Voltage:

$$V_{\text{peak}} := -V_{\text{IN}'} n \cdot \frac{(2 \cdot D_{\text{max}} - 1)}{D_{\text{max}} \cdot (D_{\text{max}} - 1)}$$

Capacitor Ca Voltage:

$$V_a := V_o + n \cdot V_{IN} \cdot \frac{(1 - D_{max})}{D_{max}}$$

Capacitor Cb Voltage:

$$V_b := n \cdot V_{IN} \cdot \frac{(1 - D_{max})}{D_{max}}$$

$$V_{b} = 24.059 V$$

3.2 - AC Output

Duty Cycle Variation - AC Output:

$$D_{AC}(\alpha) := \frac{M \cdot \sin(\alpha) - 2 + \sqrt{M^2 \cdot \sin(\alpha)^2 + 4}}{2 \cdot M \cdot \sin(\alpha)}$$

$$T_{ACp.}(\alpha) := \frac{D_{AC}(\alpha)}{f_s}$$

$$T_{ACp.}\left(\frac{\pi}{2}\right) = 37.211 \cdot \mu s$$

 $T_{ACp.}\left(\frac{3\pi}{2}\right) = 12.789 \cdot \mu s$

 $D_{AC}\left(\frac{\pi}{2}\right)$

 $D_{AC} = \frac{3\pi}{2}$

(-)

TACI

TACn

= 0.744

= 0.256

12.789-µs

37.211-µs

203.664 V

S1N (1-D) - tOFF:

$$T_{ACn}(\alpha) := \frac{1 - D_{AC}(\alpha)}{f_s}$$

Peak Positive Voltage:

$$V_{pkp}(\alpha) := \frac{D_{AC}(\alpha) \cdot V_{IN} \cdot n}{(1 - D_{AC}(\alpha))}$$

 $v_{pkN}(\alpha) \coloneqq \frac{\left(1 - D_{AC}(\alpha)\right) \cdot v_{IN'} n}{D_{AC}(\alpha)}$

$$V_{\rm pkN}\left(\frac{\pi}{2}\right) = 24.059 \, \rm V$$

 $V_{pkN}\left(\frac{3\pi}{2}\right) = 203.664 \text{ V}$

 $V_{\text{pk},\text{pk}}\left(\frac{3\pi}{2}\right) = 24.059 \text{ V}$

4 - Output Filter Capacitors

DC Output Voltage Ripple:

$$\Delta V_0 := V_0 \cdot \Delta V_{\%}$$

Capacitance:

$$\mathbf{C}_{0} \coloneqq \frac{\mathbf{I}_{0} \cdot \mathbf{D}}{\Delta \mathbf{V}_{0} \cdot \mathbf{f}_{s}}$$

AC Output Voltage:

 $\Delta V_{0 AC} := V_0 \cdot \Delta V_{\% AC}$

$$C_0 = 77.5 \ \mu F$$

 $\Delta V_{o} = 0.898 V$

 $\Delta V_{o_AC} = 52.085 V$

AC Output Cpacitance

 $C_{o_AC} := \frac{I_{o_AC} D_{max}}{\Delta V_{o_AC} f_s}$

Ca Maximum Voltage (AC):

$$V_{aAC}(\alpha) := V_{pkp}(\alpha) + \frac{\Delta V_{o_AC}}{2}$$

Cb Maximum Voltage (AC):

$$V_{bAC}(\alpha) := V_{pkN}(\alpha) + \frac{\Delta V_{o_AC}}{2}$$

5. Magnetizing Inductance 5.1 DC Operation

Mag. Inductance Average Current (DC) - LM1:

$$I_{LM}(\alpha) := \frac{I_{AC}(\alpha)}{(1 - D_{max})}$$

Mag. Inductance Average Current (DC) - LM2:

$$I_{LM2}(\alpha) := \frac{I_{AC}(\alpha)}{n \cdot (D_{max})}$$

Min Current in LM1:

$$I_{LM_min}(\alpha) := I_{LM}(\alpha) - I_{LM}(\alpha) \cdot \frac{\Delta I_{L\%}}{2}$$

Max Current in LM1:

$$\mathbf{I}_{LM_max}(\alpha) \coloneqq \mathbf{I}_{LM}(\alpha) + \mathbf{I}_{LM}(\alpha) \cdot \frac{\Delta \mathbf{I}_{L\%}}{2}$$

LM1 Current Ripple

$$I_{LM} \operatorname{delta}(\alpha) := I_{LM}(\alpha) \cdot \Delta I_{L\%}$$

Magnetizing Inductance:

$$L_{M} := \frac{V_{IN} \cdot D_{max}}{\Delta I_{L\%} I_{LM} \left(\frac{\pi}{2}\right) \cdot f_{s}}$$

$$L_M = 239.328 \cdot \mu H$$

5.2 Cálculo Operação AC

LM Current (AC):

$$I_{LM_AC}(\alpha) := \frac{I_{o_AC}}{n \cdot (1 - D_{AC}(\alpha))}$$

Min AC LM Current:

$$I_{LM_min_AC}(\alpha) := I_{LM_AC}(\alpha) - I_{LM_AC}(\alpha) \cdot \frac{\Delta I_{L\%}}{2}$$

$$I_{LM_AC}\left(\frac{\pi}{2}\right) = 21.767 \text{ A}$$

$$I_{LM_min_AC}\left(\frac{\pi}{2}\right) = 16.325 \text{ A}$$

 $V_{aAC}\left(\frac{\pi}{2}\right) = 229.707 V$

 $C_{o_AC} = 3.978 \cdot \mu F$

$$V_{bAC}\left(\frac{3\pi}{2}\right) = 229.707 V$$

$$I_{LM}\left(\frac{\pi}{2}\right) = 21.767 \text{ A}$$

$$I_{LM2}\left(\frac{3\pi}{2}\right) = -7.481 \,\mathrm{A}$$

$$I_{LM_min}\left(\frac{\pi}{2}\right) = 16.325 \text{ A}$$

$$I_{LM_max}\left(\frac{\pi}{2}\right) = 27.209 \text{ A}$$

$$I_{LM} \frac{\pi}{delta} = 10.884 \text{ A}$$

Max AC LM Current:

$$I_{LM_max_AC}(\alpha) := I_{LM_AC}(\alpha) + I_{LM_AC}(\alpha) \cdot \frac{\Delta I_{LS}}{2}$$

...

Mag. Inductance AC Current Ripple

$$I_{LM}$$
 delta $AC^{(\alpha)} := I_{LM} AC^{(\alpha)} \cdot \Delta I_{L\%}$

Indutância Magnetização:

$$L_{M_AC} := \frac{V_{IN} D_{AC} \left(\frac{\pi}{2}\right)}{\Delta I_{L\%} I_{LM_AC} \left(\frac{\pi}{2}\right) f_{s}}$$

π 2

27.209 A

= 10.884 A

ILM_max_AC

 $I_{LM_{delta}AC} \left(\frac{\pi}{2}\right)$

6 - Switches

6.1 - S1P

6.1.1 - S1P - DC Calculations

Min Current S1P::

$$I_{S1P_min} := n \cdot \frac{I_o}{(1 - D_{max})} - V_{IN} \cdot \frac{(D_{max})}{2 \cdot f_s \cdot L_M}$$

Max Current S1P:

$$I_{S1P_max} := I_{S1P_min} + V_{IN} \cdot \frac{D_{max}}{L_{M} \cdot f_s}$$

Average Current S1P:

$$I_{S1P} := \left(I_{S1P}\max + I_{S1P}\min\right) \cdot \frac{D_{max}}{2}$$

Max. Voltage - S1P:

$$\mathbf{V}_{\mathrm{S1P}_\mathrm{max}} \coloneqq \mathbf{V}_{\mathrm{IN}} + \frac{\mathbf{V}_{\mathrm{b}}}{n} + \mathbf{V}_{\mathrm{o}} \cdot \frac{1}{n}$$

 $V_{S1P_max} = 273.664 V$

 $I_{S1P_{min}} = 5.442 A$

I_{S1P_max} = 16.325 A

 $I_{S1P} = 8.1 A$

RMS Current S1P:

$$I_{S1P_ef} \coloneqq \sqrt{\frac{1}{T_s}} \left[\int_0^{D_{max} \cdot T_s} \left[\left(\frac{I_{S1P_max} - I_{S1P_min}}{D_{max} \cdot T_s} \right) t + I_{S1P_min} \right]^2 dt \right]$$

$$I_{S1P_ef} = 9.772 \text{ A}$$

6.1.2 - S1P - AC Calculations

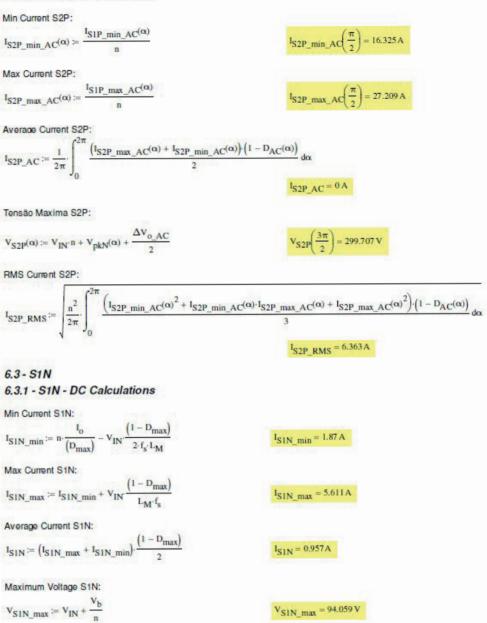
Min. Current - S1P: $I_{AC}(\alpha) \qquad \begin{pmatrix} D_{AC}(\alpha) \end{pmatrix}$

$$I_{SIP_min_AC}(\alpha) \simeq n \cdot \frac{RC}{(1 - D_{AC}(\alpha))} - V_{IN} \cdot \frac{CRC}{2 \cdot f_s \cdot L_{M_AC}}$$

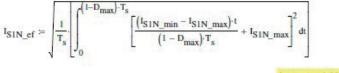
$$I_{S1P_min_AC}\left(\frac{\pi}{2}\right) = 16.325 \text{ A}$$

$$\begin{split} \text{Max. Current - S1P:} & \text{I}_{\text{S1P_max}_AC}(\alpha) \coloneqq \text{I}_{\text{S1P_max}_AC}(\alpha) + \text{V}_{\text{IN}} \frac{D_{\text{AC}}(\alpha)}{t_{\text{M}_AC}t_{\text{S}}} & \text{I}_{\text{S1P}_\text{max}_AC}\left(\frac{\pi}{2}\right) = 27.209 \text{ A} \\ \text{Average Current - S1P:} & \text{I}_{\text{S1P}_AC} \coloneqq \frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(\frac{1}{151P_\text{max}_AC}(\alpha) + \frac{1}{151P_\text{min}_AC}(\alpha)\right) D_{\text{AC}}(\alpha)}{2} d\alpha & \text{I}_{\text{S1P}_AC} \equiv 3.571 \text{ A} \\ \text{Max. Voltage - S1P:} & \text{V}_{\text{S1P}}(\alpha) \coloneqq V_{\text{IN}} + V_{\text{pkP}}(\alpha) \frac{1}{n} + \frac{\Delta V_{0_AC}}{2n} & \text{V}_{\text{S1P}}\left(\frac{\pi}{2}\right) = 299.707 \text{ V} \\ \text{RMS Current - S1P:} & \text{I}_{\text{S1P}_\text{RMS}} \coloneqq \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} \frac{\left(\frac{1}{151P_\text{min}_AC}(\alpha)^2 + \frac{1}{151P_\text{min}_AC}(\alpha) + \frac{1}{151P_\text{max}_AC}(\alpha) + \frac{1}{151P_\text{max}_AC}(\alpha)^2\right) D_{\text{AC}}(\alpha)}{3} d\alpha \\ & \text{I}_{\text{S1P}_\text{RMS}} \equiv \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} \frac{\left(\frac{1}{151P_\text{min}_AC}(\alpha)^2 + \frac{1}{151P_\text{min}_AC}(\alpha) + \frac{1}{151P_\text{max}_AC}(\alpha)^2\right) D_{\text{AC}}(\alpha)}{3} d\alpha \\ & \text{I}_{\text{S1P}_\text{RMS}} \equiv 8.941 \text{ A} \\ \textbf{6.2 - S2P} \\ \textbf{6.2.1 - S2P - DC Calculations} \\ \text{Min Current - S2P:} \\ & \text{I}_{\text{S2P}_\text{min}} = -\frac{\frac{1}{151P_\text{min}}}{n} \\ & \text{I}_{\text{S2P}_\text{min}} = -\frac{1}{5.42 \text{ A}} \\ \text{Max. Voltage - S2P:} \\ & \text{I}_{\text{S2P}_\text{max}} \coloneqq \frac{1}{152P_\text{max}} + \frac{1}{152P_\text{max}}\right) \frac{\left(1 - D_{\text{max}}\right)}{2} \\ & \text{I}_{\text{S2P}_\text{max}} \approx 273.664 \text{ V} \\ \text{RMS Current - S2P:} \\ & \text{I}_{\text{S2P}_\text{max}} \coloneqq V_0 + V_{\text{IN}}n + V_0 \\ & \text{V}_{\text{S2P}_\text{max}} \equiv \frac{273.664 \text{ V}}{2} \\ \text{RMS Current S2P:} \\ & \text{I}_{\text{S2P}_\text{max}} \coloneqq V_0 + V_{\text{IN}}n + V_0 \\ & \text{V}_{\text{S2P}_\text{max}} \cong 273.664 \text{ V} \\ \text{RMS Current S2P:} \\ & \text{I}_{\text{S2P}_\text{cf}} \coloneqq \left\{ \frac{1}{\pi_s} \left[\frac{\left(\frac{1}{1 - D_{\text{max}} \right)^{-1}_{\text{S2P}_\text{max}} \right)^{-1}_{\text{S2P}_\text{max}} \right]^{-1}_{\text{S2P}_\text{max}} \right]^{-1}_{\text{S2P}_\text{max}} \right]^{-1}_{\text{S2P}_\text{max}} \end{bmatrix} \right]^{-1}_{\text{S2P}_\text{max}} \end{bmatrix} \right]^{-1}_{\text{S2P}_\text{max}} \end{bmatrix} \right]^{-1}_{\text{S2P}_\text{max}} = 273.664 \text{ V} \\ \text{RMS Current S2P:} \\ & \text{I}_{\text{S2P}_\text{cf}} \equiv \left\{ \frac{1}{\pi_s} \left[\frac{1}{\pi_s} \left[\frac{1}{1 - D_{\text{max}}} \right]^{-1}_{\text{S2P}_\text{max}} \right]^{-1}_{\text{S2P}_\text{max}} \right]^{-1}_{\text{S2P}_\text{max}} \end{bmatrix} \right]^{-1}_{\text{S2P}_\text{max}} \end{bmatrix}$$

6.2.2 - S2P - AC Calculations



RMS Current S1N:



 $I_{SIN_{ef}} = 1.969 A$

6.3.2 - S1N - AC Calculations

Min Current S1N:

 $I_{S1N_min_AC}(\alpha) := n \cdot \frac{I_{AC}(\alpha)}{\left(D_{AC}(\alpha)\right)} - V_{IN} \cdot \frac{\left(1 - D_{AC}(\alpha)\right)}{2 \cdot f_s \cdot L_M}$

Maximum Current S1N:

$$I_{S1N_max_AC}(\alpha) := I_{S1N_min_AC}(\alpha) + V_{IN} \cdot \frac{\left(1 - D_{AC}(\alpha)\right)}{L_{M} \cdot f_{e}}$$

 $I_{S1N}_{min}AC\left(3\frac{\pi}{2}\right) = -27.209 \text{ A}$

 $I_{S1N_max_AC}\left(\frac{3\pi}{2}\right) = -16.325 \text{ A}$

299.707 V

Average Current S1N:

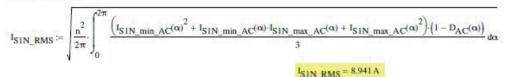
$$I_{S1N_AC} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{(I_{S1N_max_AC}(\alpha) + I_{S1N_min_AC}(\alpha)) \cdot (1 - D_{AC}(\alpha))}{2} d\alpha$$

$$I_{S1N_AC} := -3.571A$$

Tensão Maxima S1N:

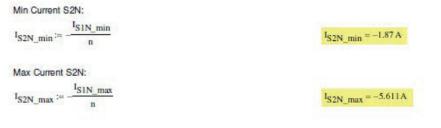
$$v_{S1N}(\alpha) := v_{IN} + \frac{v_{pkN}(\alpha)}{n} + \frac{\Delta v_{o_AC}}{2 \cdot n}$$

RMS Current S1N:

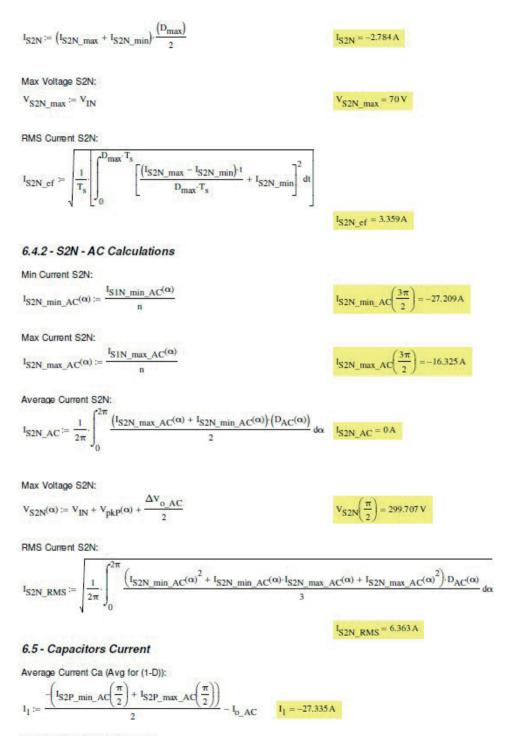


6.4 - S2N

6.4.1 - S2N - DC Calculation



Average Current S2N:



Average Current Cb (Avg for D):

$$I_2 := \frac{\left(I_{S2N_min_AC}\left(\frac{\pi}{2}\right) + I_{S2N_max_AC}\left(\frac{\pi}{2}\right)\right)}{2} + I_{0_AC} \qquad I_2 = 13.049 \text{ A}$$

6.6 - Transfer Function

$$\begin{split} & A_{s4,IN} \coloneqq L_M^{-2}C_{0,AC}^{-2,n^4}R_{0,AC} & A_{s4,IN} = 0 \frac{\sin^2 4g}{A^2} \\ & B_{s3} \coloneqq \frac{-L_M^{-2}C_{0,AC}^{-n^2}(\frac{1}{L_M}\left(\frac{\pi}{2}\right) + \frac{1}{L_M2}\left(\frac{3\pi}{2}\right))}{A_{s4,IN}} & B_{s3} \equiv -1.113 \times 10^5 \frac{A}{s} \\ & B_{s2} \coloneqq \frac{L_M^{-1}C_{0,AC}^{-n^2}(\frac{V_n - V_n \cdot D_{max} + V_{IN} \cdot n + V_b \cdot D_{max})}{A_{s4,IN}} & B_{s2} \equiv 4.559 \times 10^9 \frac{A}{s^2} \\ & B_{s2} \coloneqq \frac{-L_M^{-n}\left(D_{max}^{-2,I}L_M\left(\frac{\pi}{2}\right) + \frac{1}{L_M2}\left(\frac{3\pi}{2}\right) - 2 \cdot D_{max} \cdot \frac{1}{L_M2}\left(\frac{3\pi}{2}\right) + D_{max}^{-2,I}L_M2\left(\frac{3\pi}{2}\right)\right)}{A_{s4,IN}} & B_{s} \equiv -9.469 \times 10^{13} \frac{A}{s^3} \\ & B_{0} \coloneqq \frac{(1 - D_{max}) \cdot D_{max}\left(V_n \cdot D_{max} + V_b - V_b \cdot D_{max} + V_{IN} \cdot n\right)}{A_{s4,IN}} & B_{0} \equiv 1.483 \times 10^{18} \frac{A}{s^3} \\ & A_{44} \coloneqq \frac{L_M^{-2}C_{0,AC}^{-2,n^4} \cdot R_{0,AC}}{A_{54,IN}} & A_{s4} \equiv 1 \\ & A_{33} \coloneqq \frac{2L_M^{-2}C_{0,AC}^{-n^4} \cdot R_{0,AC}}{A_{54,IN}} & A_{s4} \equiv 1 \\ & A_{33} \coloneqq \frac{2L_M^{-2}C_{0,AC}^{-n^4} \cdot R_{0,AC}}{A_{54,IN}} & A_{s3} \equiv 1.559 \times 10^4 \frac{1}{s} \\ & A_{22} \coloneqq \frac{L_M^{-n}(D_{max}^{-2} + (1 - D_{max})^2)}{A_{54,IN}} & A_{22} = 6.505 \times 10^8 \frac{1}{s^2} \\ & A_{34,IN} & A_{34} \equiv 5.07 \times 10^{12} \frac{1}{s^3} \\ & A_{0} \coloneqq \frac{R_{0,AC}(1 - D_{max})^2 \cdot D_{max}^2}{A_{54,IN}} & A_{0} \equiv 3.999 \times 10^{16} \frac{1}{s^4} \\ & G_{ds} \coloneqq \frac{R_{33} + R_{32} + R_{3} + R_{32} + R_{3} + R_{0}}{\left(\frac{V_0}{N_{IN}}\right)^2 \cdot \sqrt{\left(\frac{V_0}{N_{IN}}\right)^2 + 4}} & K_{IIII} = 0.059 \\ \end{split}$$

APPENDIX B

APPENDIX B – CALCULATIONS FOR THE DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUTPUT CONNECTION – ALTERNATIVE SWITCHING STRATEGY

DC-AC Flyback Converter with Differential Output Connection Alternative Switching Strategy

1. Design Specifications:

Input Voltage:	$V_{IN} \approx 70V$		
RMS Output Voltage:	V _{RMS} := 127V		
Output Power:	P _o := 500W		
Switching Frequency:	f _s := 20kHz		
Mag. Inductance Current Ripple:	$\Delta I_{L\%} := 50\%$		
Output Voltage Ripple:	$\Delta V_{ m g_0} \coloneqq 0.5\%$		
AC Output Voltage Ripple	$\Delta V_{\%_AC} \approx 27.2\%$		
Relação de transformação:	$n \coloneqq 1$		
Duty Cycle (0V):	D := 0.5		
Switching Period:	$T_s := \frac{1}{f_s}$	$T_g = 50 \cdot \mu s$	

2. Preliminary Calculations:

Peak Output Voltage:

$$V_0 := V_{RMS} \sqrt{2}$$
 $V_0 = 179.605$

Modulation Index:

$$M := \frac{V_0}{V_{IN'}n}$$

2.1 - DC Calculations:

Output Current:

$$I_0 := \frac{P_0}{V_0}$$

Load Resistance:

$$R_o := \frac{V_o}{I_o}$$

 $R_0 = 64.516 \Omega$

 $I_0 = 2.784 \, A$

M = 2.566

Input Current:

$$I_e := \frac{P_o}{V_{IN}} \qquad I_e = 7.143 A$$

Output Current Ripple:

$$\Delta I_{L} := I_{0} \cdot \Delta I_{L\%} \qquad \Delta I_{L} = 1.392A$$

Output Voltage Ripple:

 $\Delta V_{o} := V_{o} \cdot \Delta V_{\mathcal{G}} \qquad \Delta V_{o} = 0.898 V$

2.2 - AC Calculations:

Output Current:

$$I_{o_AC} := \frac{2 \cdot P_o}{V_o}$$

 $I_{0_{AC}} = 5.568 A$

 $I_{AC}(\alpha) := I_0 AC^{sin(\alpha)}$

Load Resistance:

$$R_{o_AC} := \frac{V_o}{I_o AC}$$

 $R_{o_AC} = 32.258 \Omega$

Le AC = 14.286 A

Input Current:

$$I_{e_AC} := \frac{2 \cdot P_o}{V_{IN}}$$

Output Current Ripple:

$$\Delta I_{L_AC} \coloneqq I_{0_AC} \frac{\Delta I_{L\%}}{2} \qquad \Delta I_{L_AC} = 1.392A$$

3 - Output Characteristics 3.1 - DC Output

Duty Cycle:

 $D_{max} := \frac{M}{1 + M}$

D_{max} = 0.72

S1P (D) - tON:

$$T_{\max P} := \frac{D_{\max}}{f_e}$$

T_{maxP} = 35.978 μs

T_{maxN} = 14.022 μs

 $V_a = 179.605 V$

S1N (1-D) - tOFF: $T_{maxN} := \frac{1 - D_{max}}{f_e}$

Peak Output Voltage:

$$v_{pk} \coloneqq v_{IN} \cdot n \cdot \frac{D_{max}}{\sin(90 \cdot \text{deg}) \cdot (1 - D_{max})} \quad v_{pk} = 179.605 \text{ V}$$

Output Capacitor Voltage:

$$V_a := V_o$$

3.2 - AC Output

Duty Cycle Variation - AC Output (S1P):

$$D_{AC_p}(\alpha) := \begin{array}{c} \frac{M \cdot \sin(\alpha)}{1 + M \cdot \sin(\alpha)} & \text{if } \alpha < \pi \\ 0 & \text{otherwise} \end{array} \quad D_{AC_p}\left(\frac{\pi}{2}\right) = 0.72$$

Duty Cycle Variation - AC Output (S1N):

$$D_{AC_N}(\alpha) := \frac{-M \cdot \sin(\alpha)}{1 - M \cdot \sin(\alpha)} \text{ if } \pi < \alpha < 2\pi$$
0 otherwise

S1P (D) - tON:

$$T_{ACp.}(\alpha) := \frac{D_{AC_p}(\alpha)}{f_r}$$

$$T_{ACn}(\alpha) := \frac{1 - D_{AC_N}(\alpha)}{f_s}$$

$$\begin{split} \text{Peak Output Voltage - Positive Semi-cycle:} \\ V_{pkP}(\alpha) \coloneqq \frac{D_{AC_P}(\alpha) \cdot V_{IN} \cdot n}{\left(1 - D_{AC_P}(\alpha)\right)} \end{split}$$

$V_{pkP}\left(\frac{\pi}{2}\right) = 179.605 V$
$V_{pkP}\left(\frac{3\pi}{2}\right) = 0V$

= 0 V

= 179.605 V

 $V_{pkN}\left(\frac{\pi}{2}\right)$

 $T_{ACn}\left(\frac{3\pi}{2}\right)$

 $D_{AC_N}\left(\frac{3\pi}{2}\right)$

TACP.

= 0.72

35.978 µs

= 14.022·µs

$$\begin{split} \text{Peak Output Voltage - Negative Semi-Cycle:} \\ V_{pkN}(\alpha) \coloneqq \frac{D_{AC_N}(\alpha) \cdot V_{IN} \cdot n}{\left(1 - D_{AC_N}(\alpha)\right)} \end{split}$$

$$V_{aAC}(\alpha) := V_{pkp}(\alpha)$$
 if $\alpha < \pi$
0 otherwise

$$V_{aAC}\left(\frac{\pi}{2}\right) = 179.605 V$$
$$V_{aAC}\left(\frac{3\pi}{2}\right) = 0 V$$

37

Capacitor Cb - Voltage:

$$V_{bAC}(\alpha) := V_{pkN}(\alpha)$$
 if $\pi < \alpha < 2\pi$
0 otherwise

AC Output Voltage Ripple:

 $\Delta V_{o_AC} \coloneqq V_{o} \cdot \Delta V_{\%_AC}$

AC Output Voltage + Ripple:

$$\Delta V_{o_pk} \approx V_o + \frac{\Delta V_{o_AC}}{2}$$

$$V_{bAC}\left(\frac{\pi}{2}\right) = 0 V$$

 $V_{bAC}\left(\frac{3\pi}{2}\right) = 179.605 V$

 $\Delta V_{o_AC} = 48.853 V$

$\Delta V_{o pk} = 204.031 V$

4 - Output Filter Capacitor

Capacitor (DC):

$$C_0 := \frac{I_0 \cdot D}{\Delta V_0 \cdot f_s}$$

Capacitor (AC):

$$C_{o_AC} \coloneqq \frac{I_{AC}\left(\frac{\pi}{2}\right) \cdot D_{AC_P}\left(\frac{\pi}{2}\right)}{\Delta V_{o_AC} \cdot f_s}$$

Max. Voltage - Capacitor Ca (AC):

 $V_{a max}(\alpha) := V_{pkp}(\alpha) + V_{bAC}(\alpha)$

Max. Voltage - Capacitor Cb (AC):

 $V_{b_{max}}(\alpha) := V_{pkN}(\alpha) + V_{aAC}(\alpha)$

5 - Magnetizing Inductance 5.1 - DC Operation

-

Average Current:

$$I_{LM} := \frac{*o}{n \cdot (1 - D_{max})}$$

Min Current in Lm

$$I_{LM}_{min} := I_{LM} - I_{LM} \cdot \frac{\Delta I_{L\%}}{2}$$

Max Current in Lm

$$I_{LM}_{max} \coloneqq I_{LM} + I_{LM} \cdot \frac{\Delta I_{L\%}}{2}$$

Magnetizing Inductance Lm:

$$L_{M} := \frac{V_{IN} D_{max}}{\Delta I_{L\%} 2I_{LM} f_{s}}$$

...

 $I_{LM_max} = 12.408 \text{ A}$

ILM min = 7.445A

 $I_{LM} = 9.927 A$

5.2 - AC Operation

Current in Lm

$$I_{LM_AC}(\alpha) := \frac{I_{o_AC}}{n \cdot (1 - D_{AC_P}(\alpha))}$$

Max Current in Lm

$$I_{LM_min_AC}(\alpha) := I_{LM_AC}(\alpha) - I_{LM_AC}(\alpha) \cdot \frac{\Delta I_{L\%}}{2}$$

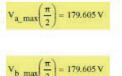
Min Current in Lm

$$\mathbf{I}_{\mathrm{LM_max_AC}}(\alpha) \coloneqq \mathbf{I}_{\mathrm{LM_AC}}(\alpha) + \mathbf{I}_{\mathrm{LM_AC}}(\alpha) \cdot \frac{\Delta \mathbf{I}_{\mathrm{L\%}}}{2}$$

$$I_{LM_AC}\left(\frac{\pi}{2}\right) = 19.853 \text{ A}$$
$$I_{LM_min_AC}\left(\frac{\pi}{2}\right) = 14.89 \text{ A}$$
$$I_{LM_max_AC}\left(\frac{\pi}{2}\right) = 24.817 \text{ A}$$

 $C_0 = 77.5 \,\mu\text{F}$





Current Ripple in Lm

$$I_{LM_delta_AC}(\alpha) := I_{LM_AC}(\alpha) \cdot \Delta I_{L\%}$$

$$I_{LM_delta_AC}\left(\frac{\pi}{2}\right) = 9.927 \text{ A}$$
Magnetizing Inductance:
$$I_{M_AC} := \frac{V_{IN} \cdot D_{AC_P}\left(\frac{\pi}{2}\right)}{\Delta I_{L\%} \cdot I_{LM_AC}\left(\frac{\pi}{2}\right) \cdot f_{s}}$$

$$I_{M_AC} = 253.704 \, \mu\text{H}$$
6 - Switches
6.1 - S1P
6.1.1 - DC Operation
Min Current
$$I_{S1P_min} := \frac{I_{b}}{D_{c}} - V_{IN} \cdot \frac{D_{max}}{2I_{Lw}f}$$

$$I_{S1P_min} = 4.963 \text{ A}$$

$$I_{S1P}min := \frac{I_e}{D_{max}} - V_{IN} \frac{D_{max}}{2 \cdot L_M \cdot f_s}$$

Max Current

$$I_{S1P_max} := I_{S1P_min} + V_{IN} \frac{D_{max}}{L_{M'}f_s}$$

$$I_{S1P} := (I_{S1P}_{max} + I_{S1P}_{min}) \cdot \frac{D_{max}}{2}$$
 $I_{S1P} = 7.143 \text{ A}$

Max Voltage

$$V_{SIP_max} \coloneqq V_{IN} + V_0 \cdot \frac{1}{n}$$
 $V_{SIP_max} = 249.605 V$

RMS Current

$$I_{S1P_ef} := \sqrt{\frac{1}{T_s}} \left[\int_0^{D_{max} \cdot T_s} \left[\left(\frac{I_{S1P_max} - I_{S1P_min}}{D_{max} \cdot T_s} \right) \cdot t + I_{S1P_min} \right]^2 dt \right]$$
$$I_{S1P_ef} = 8.764 \text{ A}$$

6.1.2 - AC Operation

Min Current

$$I_{S1P_min_AC}(\alpha) \coloneqq n \cdot \frac{I_{AC}(\alpha)}{\left(1 - D_{AC_P}(\alpha)\right)} - V_{IN} \cdot \frac{\left(D_{AC_P}(\alpha)\right)}{2 \cdot f_s \cdot L_{M_AC}}$$

Max Current

$$I_{\text{SIP}_{\text{max}_{\text{AC}}}(\alpha)} := I_{\text{SIP}_{\text{min}_{\text{AC}}}(\alpha)} + V_{\text{IN}} \frac{D_{\text{AC}_{\text{P}}}(\alpha)}{L_{\text{M}_{\text{AC}}} f_{\text{s}}}$$

$$I_{\text{S1P}_min}AC\left(\frac{\pi}{2}\right) = 14.89 \text{ A}$$
$$I_{\text{S1P}_max}AC\left(\frac{\pi}{2}\right) = 24.817 \text{ A}$$

Average Current

$$I_{S1P_{A}C} := \frac{1}{2\pi} \int_{0}^{\pi} \frac{(I_{S1P_{max},AC}(\alpha) + I_{S1P_{min},AC}(\alpha)) D_{AC_{*}P}(\alpha)}{2} d\alpha - I_{S1P_{A}C} = 3.571 A$$
Max Voltage

$$V_{S1P}(\alpha) := V_{IN} + V_{pk}p(\alpha) \frac{1}{n} + \frac{\Delta V_{\alpha,AC}}{2} V_{S1P}(\frac{\pi}{2}) = 274.031 V$$
PMS Current

$$I_{S1P_{*}RMS} := \sqrt{\frac{1}{2\pi} \int_{0}^{2\pi} \frac{(I_{S1P_{*}max_{*},AC}(\alpha)^{2} + I_{S1P_{*}max_{*},AC}(\alpha) + I_{S1P_{*}min_{*},AC}(\alpha) + I_{S1P_{*}min_{*},AC}(\alpha)^{2}) D_{AC_{*}P}(\alpha)}{3} d\alpha}$$

$$I_{S1P_{*}RMS} = 7.548 A$$
6.2 - S2P
6.2.1 - DC Operation
Min Current

$$I_{S2P_{*}min} := \frac{I_{0}}{(1 - D_{max})} - V_{IN} \frac{D_{max}}{2 \cdot I_{M} \cdot f_{s}}$$

$$I_{S2P_{*}min} = 4.963 A$$
Max Current

$$I_{S2P_{*}max} := I_{S2P_{*}min} + V_{IN} \frac{D_{max}}{I_{M} \cdot f_{s}}$$

$$I_{S2P_{*}max} = 14.89 A$$
Average Current

$$I_{S2P_{*}max} := V_{0} + V_{IN'} N$$

$$V_{S2P_{*}max} = 249.605 V$$
PMS Current

$$I_{S2P_{*}cf} := \left(\int_{0}^{1} \frac{1}{(1 - D_{max})^{-T_{s}}} \left[\frac{(I_{S2P_{*}min^{-1}S2P_{*}max})^{+1}}{(1 - D_{max})^{-T_{s}}} + I_{S2P_{*}max} \right]^{2} dt \right]$$

$$I_{S2P_{*}cf} := \int_{0}^{1} \frac{1}{(1 - D_{max})^{-T_{s}}} \left[\frac{(I_{S2P_{*}min^{-1}S2P_{*}max})^{+1}}{(1 - D_{max})^{-T_{s}}} + I_{S2P_{*}max} \right]^{2} dt$$

6.2.2 - AC Operation

Min Current

$$\label{eq:IS2P_min_AC} \begin{split} & \text{I}_{AC}(\alpha) \coloneqq \frac{\text{I}_{AC}(\alpha)}{\left(1 - \text{D}_{AC_P}(\alpha)\right)} - \text{V}_{IN} \cdot \frac{\text{D}_{AC_P}(\alpha)}{2 \cdot \text{L}_M \cdot f_s} \end{split}$$

 $I_{S2P_min_AC}\left(\frac{\pi}{2}\right) = 14.89 A$

Max Current

$$I_{S2P_max_AC}(\alpha) := I_{S2P_min_AC}(\alpha) + V_{IN'} \frac{D_{AC_P}(\alpha)}{L_{M'}f_s}$$

$$I_{S2P_max_AC}\left(\frac{\pi}{2}\right) = 24.817 \text{ A}$$
Average Current
$$I_{S2P_AC} := \frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{S2P_max_AC}(\alpha) + I_{S2P_min_AC}(\alpha)\right) \cdot \left(1 - D_{AC_P}(\alpha)\right)}{2} d\alpha \qquad I_{S2P_AC} = 0 \text{ A}$$
Max Voltage
$$V_{S2P}(\alpha) := V_{IN'}n + V_{pkP}(\alpha) + \frac{\Delta V_{0_AC}}{2}$$

$$V_{S2P}\left(\frac{\pi}{2}\right) = 274.031 \text{ V}$$
RMS Current:
$$I_{COP_max_AC}\left(\alpha\right)^{2} + I_{S2P_max_AC}(\alpha) \cdot I_{S2P_min_AC}(\alpha) + I_{S2P_min_AC}(\alpha)^{2} \cdot \left(1 - D_{AC_P}(\alpha)\right) d\alpha$$

$$I_{S2P_{RMS}} := \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} \frac{\left(I_{S2P_{max_{AC}}(\alpha)}^{2} + I_{S2P_{max_{AC}}(\alpha)} \cdot I_{S2P_{min_{AC}}(\alpha)} + I_{S2P_{min_{AC}}(\alpha)}^{2}\right) \cdot \left(1 - D_{AC_{P}(\alpha)}\right)}{3} d\alpha$$

$$I_{S2P_{RMS}} = 5.777 \text{ A}$$

6.3 - Função Transferencia Corrente

$$\begin{split} & A_{s4_IN} \coloneqq n^{4} \cdot R_{o_AC'} L_{M}^{2} \cdot C_{o_AC}^{2} \\ & B_{s3} \coloneqq \frac{-n^{3} \cdot L_{M}^{-2} \cdot C_{o_AC'} l_{LM_AC} \left(\frac{\pi}{2}\right)}{A_{s4_IN}} \\ & B_{s2} \coloneqq \frac{n^{2} \cdot \left(1 - D_{max}\right) \cdot L_{M} \cdot C_{o_AC'} \left(V_{IN} \cdot n + V_{a}\right)}{A_{s4_IN}} \\ & B_{s1} \coloneqq \frac{-n \cdot L_{M} \cdot l_{LM_AC} \left(\frac{\pi}{2}\right)}{A_{s4_IN}} \\ & B_{0} \coloneqq \frac{\left(1 - D_{max}\right) \cdot \left(V_{IN} \cdot n + V_{a}\right)}{A_{s4_IN}} \\ & A_{s4} \coloneqq \frac{n^{4} \cdot R_{o_AC'} L_{M}^{-2} \cdot C_{o_AC'}^{2}}{A_{s4_IN}} \\ & A_{s3} \coloneqq \frac{2 \cdot n^{4} \cdot L_{M}^{-2} \cdot C_{o_AC}}{A_{s4_IN}} \\ & A_{s2} \coloneqq \frac{n^{2} \cdot R_{o_AC'} L_{M} \cdot C_{o_AC} \left(D_{max}^{-2} - 2 \cdot D_{max} + 2\right)}{A_{s4_IN}} \\ \end{split}$$

$$A_{s4_IN} = 0 \frac{s \cdot m^2 \cdot kg}{A^2}$$

$$B_{s3} = -1.501 \times 10^5 \frac{A}{s}$$

$$B_{s2} = 2.086 \times 10^9 \frac{A}{s^2}$$

$$B_{s1} = -1.443 \times 10^{14} \frac{A}{s^3}$$

$$B_0 = 2.005 \times 10^{18} \frac{A}{s^4}$$

$$A_{s4} = 1$$

$$A_{s3} = 1.512 \times 10^4 \frac{1}{s}$$

$$A_{s2} = 1.037 \times 10^9 \frac{1}{s^2}$$

$$A_{s1} := \frac{n^2 L_{M'} (D_{max}^2 - 2 \cdot D_{max} + 2)}{A_{s4_IN}}$$
$$A_0 := \frac{R_{o_AC'} (D_{max}^2 - 2 \cdot D_{max} + 1)}{A_{s4_IN}}$$

$$A_{s1} = 7.839 \times 10^{12} \frac{1}{s^3}$$
$$A_0 = 7.267 \times 10^{16} \frac{1}{s^4}$$

$$G_{ds} := \frac{B_{s3} + B_{s2} + B_{s} + B_{0}}{A_{s4} + A_{s3} + A_{s2} + A_{s} + A_{0}}$$

$$K_{\text{lin}} \coloneqq \frac{1}{\left[1 + \frac{n \cdot \left(V_{aAC}\left(\frac{\pi}{2}\right) - V_{bAC}\left(\frac{\pi}{2}\right)\right)}{V_{IN}}\right]^2}$$

$$K_{\text{lin}} = 0.079$$

Appendix B 194

APPENDIX C

APPENDIX C - CALCULATION OF LOSSES FOR THE DC-AC FLYBACK CONVERTERWITHDIFFERENTIAL OUTPUTCONNECTION-COMPLEMENTARY **SWITCHING**

DC-AC Flyback Converter with Differential Output Connection - Calculation of Losses

Specifications:

 $P_{o} := 500W$

 $V_{TM} := 70V$

V_{RMS} := 127V

 $f_{z} := 20 \text{kHz}$

 $L_{M} := 253.715 \mu H$

n := 1

Peak Output Voltage:

 $V_o := \sqrt{2} \cdot V_{RMS}$

Output Current: $I_{o_pk} := \frac{2 \cdot P_o}{V_o}$

 $I_o(\alpha) := I_o \text{ pk} \cdot \sin(\alpha)$

Modulation Index: $M := \frac{n \cdot V_o}{V_{IN}}$

Load Resistance:

 $R_o := \frac{V_o}{I_o pk}$

 $R_0 = 32.258 \Omega$

V_{o_neg_pk} = 203.664 V

M = 2.566

 $V_0 = 179.605 V$

I_{o pk} = 5.568 A

Duty Cycle:

$$D(\alpha) := \frac{M \cdot \sin(\alpha) - 2 + \sqrt{M^2 \cdot \sin(\alpha)^2 + 4}}{2 \cdot M \cdot \sin(\alpha)}$$

Output Voltages (Peak Positive and Negative): $V_{o_pos}(\alpha) := \frac{D(\alpha)}{n \cdot (1 - D(\alpha))} \cdot V_{IN}$ $V_{o_pos_pk} := V_{o_pos}\left(\frac{\pi}{2}\right)$ V_{o pos pk} = 203.664 V $V_{o_neg}(\alpha) := \frac{(1 - D(\alpha))}{n \cdot D(\alpha)} \cdot V_{IN}$ $V_{o_neg_pk} := V_{o_neg} \left(\frac{3\pi}{2}\right)$

Magnetizing Inductance Current:

$$I_{LM}(\alpha) := \frac{I_0(\alpha)}{n \cdot (1 - D(\alpha))}$$

Magnetizing Inductance - Current Ripple:

$$\Delta I_{LM}(\alpha) := \frac{D(\alpha) \cdot V_{IN}}{f_{5} \cdot L_{M}}$$
$$\Delta I_{LM_{max}} := \Delta I_{LM} \left(\frac{\pi}{2}\right) \qquad \Delta I_{LM_{max}} = 10.266 \text{ A}$$

Magnetizing Inductances' Maximum and Minimum Currents:

$$\begin{split} I_{\text{LMI}_\min}(\alpha) &\coloneqq \frac{2\mathbf{f}_{5} \cdot \mathbf{L}_{\text{M}} \cdot \mathbf{I}_{0}(\alpha) - \mathbf{D}(\alpha) \cdot (1 - \mathbf{D}(\alpha)) \cdot \mathbf{n} \cdot \mathbf{V}_{\text{IN}}}{2\mathbf{f}_{5} \cdot \mathbf{L}_{\text{M}} \cdot \mathbf{n} \cdot (1 - \mathbf{D}(\alpha))} \\ I_{\text{LMI}_\max}(\alpha) &\coloneqq \frac{2\mathbf{f}_{5} \cdot \mathbf{L}_{\text{M}} \cdot \mathbf{I}_{0}(\alpha) + \mathbf{D}(\alpha) \cdot (1 - \mathbf{D}(\alpha)) \cdot \mathbf{n} \cdot \mathbf{V}_{\text{IN}}}{2\mathbf{f}_{5} \cdot \mathbf{L}_{\text{M}} \cdot \mathbf{n} \cdot (1 - \mathbf{D}(\alpha))} \\ \end{split}$$

$$I_{\text{LM2}_{\text{max}}}(\alpha) := -\frac{2f_{\text{s}}\cdot L_{\text{M}}\cdot I_{\text{o}}(\alpha) - D(\alpha) \cdot (1 - D(\alpha)) \cdot n \cdot V_{\text{IN}}}{2f_{\text{s}}\cdot L_{\text{M}}\cdot n \cdot D(\alpha)}$$

 $\mathbf{I}_{\mathrm{LM2_min}}(\alpha) \coloneqq -\frac{2\mathbf{f}_{\mathrm{s}} \mathbf{L}_{\mathrm{M}} \mathbf{I}_{\mathrm{o}}(\alpha) + \mathbf{D}(\alpha) \cdot (1 - \mathbf{D}(\alpha)) \cdot \mathbf{n} \cdot \mathbf{V}_{\mathrm{IN}}}{2\mathbf{f}_{\mathrm{s}} \cdot \mathbf{L}_{\mathrm{M}} \cdot \mathbf{n} \cdot \mathbf{D}(\alpha)}$

Switches' Average Current Values:

$$\begin{split} & I_{\text{S1P}_\text{avg}} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{\text{LM1}_\text{min}}(\alpha) + I_{\text{LM1}_\text{max}}(\alpha)\right) \cdot D(\alpha)}{2} \, d\alpha \qquad I_{\text{S1P}_\text{avg}} = 3.571 \, \text{A} \\ & I_{\text{S2P}_\text{avg}} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{\text{LM1}_\text{min}}(\alpha) + I_{\text{LM1}_\text{max}}(\alpha)\right) \cdot (1 - D(\alpha))}{2} \, d\alpha \quad I_{\text{S2P}_\text{avg}} = 0 \, \text{A} \\ & I_{\text{S1N}_\text{avg}} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{\text{LM2}_\text{min}}(\alpha) + I_{\text{LM2}_\text{max}}(\alpha)\right) \cdot (1 - D(\alpha))}{2} \, d\alpha \quad I_{\text{S1N}_\text{avg}} = 3.571 \, \text{A} \\ & I_{\text{S1N}_\text{avg}} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{\text{LM2}_\text{min}}(\alpha) + I_{\text{LM2}_\text{max}}(\alpha)\right) \cdot (1 - D(\alpha))}{2} \, d\alpha \quad I_{\text{S1N}_\text{avg}} = 3.571 \, \text{A} \\ & I_{\text{S2N}_\text{avg}} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{\text{LM2}_\text{min}}(\alpha) + I_{\text{LM2}_\text{max}}(\alpha)\right) \cdot D(\alpha)}{2} \, d\alpha \quad I_{\text{S2N}_\text{avg}} = 0 \, \text{A} \end{split}$$

Switches' Effective Current Values:

$$I_{\text{S1P}_{\text{RMS}}} \coloneqq \sqrt{\frac{1}{2\pi}} \cdot \int_{0}^{2\pi} \frac{\left(I_{\text{LM1}_{\text{min}}}(\alpha)^{2} + I_{\text{LM1}_{\text{max}}}(\alpha) \cdot I_{\text{LM1}_{\text{min}}}(\alpha) + I_{\text{LM1}_{\text{max}}}(\alpha)^{2}\right) \cdot D(\alpha)}{3} \, d\alpha$$

$$I_{\text{S1P}_{\text{RMS}}} \equiv 8.922 \, \text{A}$$

$$\begin{split} I_{\text{S2P},\text{RMS}} &= \sqrt{\frac{n^2}{2\pi}} \int_{0}^{2\pi} \frac{\left(I_{\text{LM}_{\text{L},\text{min}}(\omega)}^2 + I_{\text{LM}_{\text{L},\text{min}}(\omega)} \cdot I_{\text{LM}_{\text{L},\text{max}}(\omega)} + I_{\text{LM}_{\text{L},\text{max}}(\omega)}^2\right) \cdot (1 - D(\omega))}{3} \, d\alpha \\ I_{\text{S2P},\text{RMS}} &= 6.346 \text{A} \end{split}$$

$$I_{\text{S1N},\text{RMS}} &= \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} \frac{\left(I_{\text{LM}_{\text{L},\text{min}}(\omega)}^2 + I_{\text{LM}_{\text{L},\text{min}}(\omega)} \cdot I_{\text{LM}_{\text{L},\text{max}}(\omega)} + I_{\text{LM}_{\text{L},\text{max}}(\omega)}^2\right) \cdot (1 - D(\omega))}{3} \, d\alpha \\ I_{\text{S1N},\text{RMS}} &= 8.922 \text{A} \end{aligned}$$

$$I_{\text{S1N},\text{RMS}} &= \frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{\text{LM}_{\text{L},\text{min}}(\omega)}^2 + I_{\text{LM}_{\text{L},\text{min}}(\omega)} \cdot I_{\text{LM}_{\text{L},\text{max}}(\omega)} + I_{\text{LM}_{\text{L},\text{max}}(\omega)}^2\right) \cdot D(\omega)}{3} \, d\alpha \\ I_{\text{S1N},\text{RMS}} &= 8.922 \text{A} \end{aligned}$$

$$I_{\text{S1N},\text{RMS}} &= \frac{1}{2\pi} \int_{0}^{2\pi} \frac{\left(I_{\text{LM}_{\text{L},\text{min}}(\omega)^2 + I_{\text{LM}_{\text{L},\text{max}}(\omega)} \cdot I_{\text{LM}_{\text{L},\text{max}}}(\omega)^2\right) \cdot D(\omega)}{3} \, d\alpha \\ I_{\text{S1N},\text{RMS}} &= 6.346 \text{A} \end{aligned}$$

$$I_{\text{S1N},\text{RMS}} &= I_{\text{S1N},\text{RMS}} = I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T1},\text{prim},\text{RMS}} &= I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T1},\text{prim},\text{RMS}} &= I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T1},\text{prim},\text{RMS}} &= I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T1},\text{prim},\text{RMS}} &= I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T1},\text{prim},\text{RMS}} &= I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T2},\text{prim},\text{RMS}} &= I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T2},\text{prim},\text{RMS}} &= I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T2},\text{prim},\text{RMS}} &= I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T2},\text{prim},\text{RMS}} = I_{\text{S1N},\text{RMS}} \qquad I_{\text{T1},\text{prim},\text{RMS}} = 8.922 \text{A} \\ I_{\text{T1},\text{prim},\text{RMS}} = I_{\text{S1N},\text{prim}, \left\{\frac{\pi}{2}\right\} \qquad I_{\text{LM},\text{prim},\text{RMS}} = 2.69 \text{A} \\ I_{\text{LM},\text{prim},\text{RMS}} = I_{\text{LM},\text{prim},\text{RMS}} = 2.69 \text{A} \\ I_{\text{LM},\text{prim},\text{S}} = I_{\text{LM},\text{prim},\text{S}} = 2.69 \text{A} \\ I_{\text{LM},\text{prim},\text{S}} = 1.00 \text{prim}, \left\{\frac{\pi}{2}\right\} \qquad I_{\text$$

$$\begin{split} V_{\text{S1P}}(\alpha) &\coloneqq V_{\text{IN}} + n \cdot V_{o_\text{pos}}(\alpha) \\ V_{\text{S1P}_\text{max}} &\coloneqq V_{\text{S1P}}\left(\frac{\pi}{2}\right) & V_{\text{S1P}_\text{max}} = 273.664 \text{ V} \\ V_{\text{S2P}}(\alpha) &\coloneqq \frac{V_{\text{D1}}}{n} + V_{o_\text{pos}}(\alpha) \\ V_{\text{S2P}_\text{max}} &\coloneqq V_{\text{S2P}}\left(\frac{\pi}{2}\right) & V_{\text{S2P}_\text{max}} = 273.664 \text{ V} \\ V_{\text{S1N}}(\alpha) &\coloneqq V_{\text{D1}} + n \cdot V_{o_\text{neg}}(\alpha) \\ V_{\text{S1N}_\text{max}} &\coloneqq V_{\text{S1N}}\left(\frac{3\pi}{2}\right) & V_{\text{S1N}_\text{max}} = 273.664 \text{ V} \end{split}$$

$$\begin{split} & V_{\text{S2N}}(\alpha) := \frac{V_{\text{IN}}}{n} + V_{\text{o_neg}}(\alpha) \\ & V_{\text{S2N}_\text{max}} := V_{\text{S2N}} \left(\frac{3\pi}{2} \right) \end{split}$$

V_{S2N_max} = 273.664 V

Calculation of Losses:

 $V_{TH0IGBT} := 1.25V$ $R_{onIGBT} := 0.01\Omega$ $V_{TH0D} := 0.98V$ $R_{D} := 0.022\Omega$

For Rg = 15 Ω

$$\begin{split} \mathbf{k_{on1}} &\coloneqq 1.75 \cdot 10^{-5} \frac{J}{A} \\ \mathbf{k_{on2}} &\coloneqq 3.75 \cdot 10^{-7} \frac{J}{A^2} \\ \mathbf{k_{off1}} &\coloneqq 6.75 \cdot 10^{-6} \frac{J}{A} \\ \mathbf{k_{off2}} &\coloneqq 1.125 \cdot 10^{-7} \frac{J}{A^2} \\ \mathbf{V_{CEref}} &\coloneqq 400 \mathbf{V} \\ \mathbf{E_{on}}(\mathbf{I_C}, \mathbf{V_{CE}}) &\coloneqq \left(\mathbf{k_{on1}} \cdot \mathbf{I_C} + \mathbf{k_{on2}} \cdot \mathbf{I_C}^2\right) \cdot \frac{\mathbf{V_{CE}}}{\mathbf{V_{CEref}}} \\ \mathbf{E_{off}}(\mathbf{I_C}, \mathbf{V_{CE}}) &\coloneqq \left(\mathbf{k_{off1}} \cdot \mathbf{I_C} + \mathbf{k_{off2}} \cdot \mathbf{I_C}^2\right) \cdot \frac{\mathbf{V_{CE}}}{\mathbf{V_{CEref}}} \\ \end{split}$$

$P_{\text{S1P_cond}} \coloneqq V_{\text{TH0IGBT}} I_{\text{S1P_avg}} + R_{\text{onIGBT}} I_{\text{S1P_RMS}}^2$	$P_{S1P_cond} = 5.26 W$
$P_{S2P_cond} \coloneqq V_{TH0IGBT}I_{S2P_avg} + R_{onIGBT}I_{S2P_RMS}^{2}$	$P_{S2P_cond} = 0.403 W$
$P_{\text{S1N}_\text{cond}} \coloneqq V_{\text{TH0IGBT}} I_{\text{S1N}_\text{avg}} + R_{\text{onIGBT}} I_{\text{S1N}_\text{RMS}}^2$	$P_{S1N_{cond}} = 5.26 W$
PS2N_cond := VTH0IGBT IS2N_avg + RonIGBT IS2N_RMS ²	$P_{\text{S2N_cond}} = 0.403 \text{W}$
$P_{SW_cond} \coloneqq P_{S1P_cond} + P_{S2P_cond} + P_{S1N_cond} + P_{S2N_cond}$	$P_{SW_cond} = 11.326 W$

 $\mathbb{E}_{\texttt{S1P}_\texttt{sw}}(\alpha) \coloneqq \mathbb{E}_{\texttt{on}}(\mathbb{I}_{\texttt{LM1}_\texttt{min}}(\alpha), \mathbb{V}_{\texttt{S1P}}(\alpha)) + \mathbb{E}_{\texttt{off}}(\mathbb{I}_{\texttt{LM1}_\texttt{max}}(\alpha), \mathbb{V}_{\texttt{S1P}}(\alpha))$

$$P_{\text{S1P}_\text{sW}} \coloneqq \frac{f_{\text{s}}}{2\pi} \cdot \int_{0}^{\pi} E_{\text{S1P}_\text{sW}}(\alpha) \, d\alpha \qquad \qquad P_{\text{S1P}_\text{sW}} = 2.028 \, \text{W}$$

$E_{S2P_{sw}}(\alpha) := E_{on}(\alpha)$	$I_{LM1_{min}}(\alpha)$, $V_{S2P}(\alpha)$	+ $E_{off}(n I_{LM1_{max}}(\alpha) , V_{S2P}(\alpha))$
--	---	---

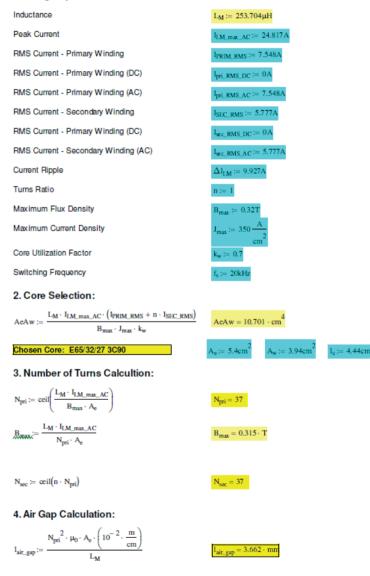
$$\begin{split} P_{S2P_{sw}} &:= \frac{f_s}{2\pi} \cdot \int_{\pi}^{2\pi} E_{S2P_{sw}}(\alpha) \, d\alpha & P_{S2P_{sw}} = 0.448 W \\ E_{S1N_{sw}}(\alpha) &:= E_{on} (I_{LM2_{min}}(\alpha), V_{S1N}(\alpha)) + E_{off} (I_{LM2_{max}}(\alpha), V_{S1N}(\alpha)) \\ P_{S1N_{sw}} &:= \frac{f_s}{2\pi} \cdot \int_{\pi}^{2\pi} E_{S1N_{sw}}(\alpha) \, d\alpha & P_{S1N_{sw}} = 2.028 W \\ E_{S2N_{sw}}(\alpha) &:= E_{on} (n | I_{LM2_{min}}(\alpha)|, V_{S2N}(\alpha)) + E_{off} (n | I_{LM2_{max}}(\alpha)|, V_{S2N}(\alpha)) \\ P_{S2N_{sw}} &:= \frac{f_s}{2\pi} \cdot \int_{0}^{\pi} E_{S2N_{sw}}(\alpha) \, d\alpha & P_{S2N_{sw}} = 0.448 W \\ P_{SW_{sw}} &:= P_{S1P_{sw}} + P_{S2P_{sw}}(\alpha) \, d\alpha & P_{S2N_{sw}} = 0.448 W \\ P_{SW_{sw}} &:= P_{S1P_{sw}} + P_{S2P_{sw}}(\alpha) \, d\alpha & P_{S2N_{sw}} = 0.448 W \\ P_{SW_{sw}} &:= P_{S1P_{sw}} + P_{S2P_{sw}}(\alpha) \, d\alpha & P_{S2N_{sw}} = 0.448 W \\ P_{SW_{sw}} &:= P_{S1P_{sw}} + P_{S2P_{sw}} + P_{S1N_{sw}} + P_{S2N_{sw}} & P_{SW_{sw}} = 4.952 W \\ P_{SW_{sw}} &:= P_{SW_{sw}} + P_{SW_{sound}} & P_{SW_{sw}} = 4.952 W \\ P_{SW_{stat}} &:= P_{SW_{sw}} + P_{SW_{sound}} & P_{SW_{sound}} = 16.278 W \\ R_{cu1} &:= 86.10^{-3} \cdot \Omega \\ R_{cu2} &:= 110 \cdot 10^{-3} \cdot \Omega \\ P_{T1_{cond}} &:= R_{cu1} \cdot I_{T2_{sw}m_{sm}} R_{MS}^{2} + R_{cu2} \cdot I_{T2_{sw}} R_{MS}^{2} & P_{T1_{cond}} = 11.276 W \\ P_{T2_{cond}} &:= R_{cu1} \cdot I_{T2_{sw}m_{sm}} R_{MS}^{2} + R_{cu2} \cdot I_{T2_{sw}} R_{MS}^{2} & P_{T2_{cond}} = 11.276 W \\ P_{T1_{sumg}} &:= 1.434W \\ P_{T2_{sumg}} &:= 1.434W \\ P_{T_{sumg}} &:= 1.434W \\ P_{clamp} &:= \frac{1.434W}{0} \\ P_{clamp} &:= 13.656 W \\ \frac{Efficiency Estimative:}{0} : n &:= \frac{P_{0}}{P_{0} + P_{SW_{stat}} + P_{T_{stat}} + 4P_{clamp}} \\ n &:= \frac{P_{0}}{P_{0} + P_{SW_{stat}} + P_{T_{stat}} + 4P_{clamp}} \\ n &:= 83.847.86 \\ \end{array}$$

APPENDIX D

APPENDIX D – DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUTPUT CONNECTION - COUPLED INDUCTOR

DC-AC Flyback Converter with Differential Output Connection - Coupled Inductor

1. Design Specifications:



5. Wire Gauge Calculation:

T_{max} := 100 $n_w := 0.8$ $\rho_T := 17.9 \cdot 10^{-9} \cdot [1 + 0.0039(T_{max} - 20)] \cdot \Omega \cdot m$ $\delta_w := \sqrt{\frac{\rho_T}{\pi \cdot \mu_0 \cdot f_r}}$ $\delta_w = 0.545 \cdot mm$ $D_{fin} := 2 \cdot \delta_w$ $D_{fio} = 0.109 \cdot cm$ Wire Gauge: The wire gauge chosen is the 29AWG. d_w := 0.29mm $d_{w iso} := 0.33 \text{mm}$ $S_{winv} := 0.000642 \cdot cm^2$ $S_{wint iso} \approx 0.000872 \cdot cm^2$ $S_{cu_prim} := \frac{I_{PRIM_RMS}}{J_{max}}$ $S_{cu, prim} = 0.022 \cdot cm^2$ $n_{cond_pri} := ceil\left(\frac{S_{cu_prim}}{S_{wire}}\right)$ n_{cond_pri} = 34 $S_{cu_sec} := \frac{I_{SEC_RMS}}{J_{max}}$ $S_{cu} = 0.017 \cdot cm^2$ $n_{cond_sec} := ceil\left(\frac{S_{cu_sec}}{S_{wine}}\right)$ n_{cond sec} = 26 6. Calculation of Losses:

6.1 Copper Calculation:

$$\begin{split} N_{campri} &\coloneqq \frac{N_{pri} \cdot n_{cond_pri} \cdot d_{w_iso}}{\eta_{w} \cdot l_{c}} \\ N_{camsec} &\coloneqq \frac{N_{pri} \cdot n_{cond_pri} \cdot d_{w_iso}}{\eta_{w} \cdot l_{c}} \\ \rho_{wire} &\coloneqq \frac{\rho_{T}}{S_{wire}} \end{split}$$

lmean_tum := 15cm

 $l_{wine_pri} := N_{pri} \cdot l_{mean_turn}$

 $R_{ccpri} \coloneqq \frac{\rho_{wine} \cdot l_{mean_turn} \cdot N_{pri}}{n_{cond_pri}}$

 $l_{wine_sec} := N_{sec} \cdot l_{mean_turn}$

$$N_{campri} = 11.688$$

$$N_{camsec} = 11.688$$

$$\rho_{wire} = 3.658 \times 10^{-3} \cdot \frac{\Omega}{cm}$$

$$l_{wire_pri} = 5.55 \text{ m}$$

$$R_{ccpri} = 0.06 \cdot \Omega$$

$$l_{wire_prc} = 5.55 \text{ m}$$

$$\begin{split} R_{\text{ccsec}} &\coloneqq \frac{p_{\text{wire}} \cdot l_{\text{mean_turn}} \cdot N_{\text{sec}}}{n_{\text{cond_sec}}} \\ \Delta &\coloneqq \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \cdot \frac{d_{w}}{\delta_{w}} \cdot \sqrt{\eta_{w}} \\ \Delta & = 0.397 \end{split}$$

$$F_{\text{rpri}} \coloneqq \Delta \cdot \left[\frac{e^{2\Delta} - e^{-2\Delta} + 2 \cdot \sin(2 \cdot \Delta)}{e^{2\Delta} + e^{-2\Delta} - 2 \cdot \cos(2 \cdot \Delta)} + \frac{2}{3} \cdot \left(N_{\text{campri}}^2 - 1 \right) \cdot \frac{e^{\Delta} - e^{-\Delta} - 2 \cdot \sin(\Delta)}{e^{\Delta} + e^{-\Delta} + 2 \cdot \cos(\Delta)} \right]$$

F_{rpri} = 1.375

$$F_{\text{nec}} \coloneqq \Delta \cdot \left[\frac{e^{2 \cdot \Delta} - e^{-2 \cdot \Delta} + 2 \cdot \sin(2 \cdot \Delta)}{e^{2 \cdot \Delta} + e^{-2 \cdot \Delta} - 2 \cdot \cos(2 \cdot \Delta)} + \frac{2}{3} \cdot \left(N_{\text{camsec}}^2 - 1 \right) \cdot \frac{e^{\Delta} - e^{-\Delta} - 2 \cdot \sin(\Delta)}{e^{\Delta} + e^{-\Delta} + 2 \cdot \cos(\Delta)} \right]$$

 $F_{\text{rsec}} = 1.375$

$$\begin{split} R_{acpri} &:= F_{ppri} \cdot R_{ccpri} & R_{acpri} = 0.082 \cdot \Omega \\ R_{acsec} &:= F_{ppri} \cdot R_{ccsec} & R_{acsec} = 0.107 \cdot \Omega \\ P_{cu_pri} &:= R_{acpri} \cdot I_{pri_RMS_AC}^2 + R_{ccpri} \cdot I_{pri_RMS_DC}^2 & P_{cu_pri} = 4.679 \cdot W \\ P_{cu_sec} &:= R_{acsec} \cdot I_{sec_RMS_AC}^2 + R_{ccsec} \cdot I_{sec_RMS_DC}^2 & P_{cu_sec} = 3.584 \cdot W \\ P_{copper} &:= P_{cu_pri} + P_{cu_sec} & P_{copper} = 8.263 \cdot W \end{split}$$

Pcopper := Pcu_pri + Pcu_sec

6.2 Magnetic Losses:

$$\begin{split} V_{cone} &:= 23.3 \, cm^3 & k \coloneqq 3.74 \, \frac{W}{m^3} & \alpha := 1.45 & \beta := 3.03 \\ \Delta t_1 &:= \frac{1}{2 \cdot 20000} & \Delta t_2 := \frac{1}{2 \cdot 20000} \end{split}$$

$$\begin{split} \Delta B &:= \frac{L_M \cdot \Delta I_{LM}}{N_{pri} \cdot A_e} \cdot \frac{1}{T} \\ P_{cone} &:= k \cdot \left(\frac{f_e}{Hz}\right)^{\text{CC}} \cdot \left(\frac{1}{2} \cdot \Delta B\right)^{\text{CC}} \cdot V_{core} \\ \end{split}$$

$$\begin{split} \mathbf{k}_{i} &:= \frac{\mathbf{k}}{\left(2 \cdot \pi\right)^{\alpha - 1} \cdot 2^{\beta - \alpha} \cdot \int_{0}^{2\pi} \left(\left|\cos(\theta)\right|\right)^{\alpha} d\theta} \\ \mathbf{P}_{v} &:= \left(\frac{\mathbf{f}_{s}}{Hz}\right) \cdot \mathbf{k}_{i} \cdot \left(\Delta B\right)^{\beta - \alpha} \cdot \left[\int_{0}^{\Delta t_{i}} \left(\frac{\Delta B}{\Delta t_{i}}\right)^{\alpha} dt + \int_{0}^{\Delta t_{2}} \left(\frac{\Delta B}{\Delta t_{2}}\right)^{\alpha} dt\right] \\ \end{split}$$

Poor Pv · Vcore

6.3 Total Losses:

 $P_{total} := P_{copper} + P_{core}$

 $P_{total} = 8.295 \cdot W$

6.4 Core Thermal Resistance:

$$Rt_{core} := 23 \cdot \frac{K}{W} \left(\frac{A_e A_w}{cm} \right)^{-0.37} \qquad Rt_{core} = 7.42 \cdot \frac{K}{W}$$

6.5 Temperature Elevation:

 $\Delta T := \left(P_{copper} + P_{core} \right) Rt_{core}$

 $\Delta T = 61.547 \text{ K}$

7. Execution:

$A_{w min} := \frac{N_{pri} \cdot S_{wire_{iso}}}{N_{pri} \cdot S_{wire_{iso}}}$	$n_{cond_pri} + N_{sec} \cdot S_{wire_iso} \cdot n_{co}$	$A_{w_min} = 2.765 \cdot cm^2$
	k _w	
Exec := $\frac{A_{w_min}}{A_w}$		Exec = 0.702

APPENDIX E

APPENDIX E – CALCULATION OF LOSSES FOR THE DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUTPUT CONNECTION – ALTERNATIVE SWITCHING

Cálculo de Perdas Conversor Flyback CC-CA Bidirecional de 500W 20kHz 127V com Modulador Alternativo

Especificações:	
$P_o := 500 W$	
V _{in} := 70V	
V _{oef} := 127V	
$\mathbf{f}_{s} := 20 \mathrm{kHz}$	
L _m := 253.715µH	
n := 1	
Valor de Pico da Tensão de Saída:	
$V_{omax} := \sqrt{2} \cdot V_{oef}$	V _{omax} = 179.605 V
Corrente de Saída (Carga Resistiva ou Interliga	do à Rede <u>):</u>
$I_{omax} := \frac{2 \cdot P_o}{V_{omax}}$	I _{omax} = 5.568 A
$I_o(\alpha) := I_{omax} \cdot \sin(\alpha)$	
Índice de Modulação:	
$M := \frac{n \cdot V_{omax}}{V_{in}}$	M = 2.566
Resistência Equivalente de Saída:	
$R_o := \frac{V_{omax}}{I_{omax}}$	$R_0 = 32.258 \Omega$
Função Razão Cíclica:	

 $D_{p}(\alpha) := \begin{array}{c} \frac{M \cdot \sin(\alpha)}{1 + M \cdot \sin(\alpha)} & \text{if } \alpha < \pi \\ 0 & \text{otherwise} \end{array}$

Valores de Tensão de Saída "p" e "n":

$$\begin{split} & V_{op}(\alpha) := \frac{D_p(\alpha)}{n \cdot (1 - D_p(\alpha))} \cdot V_{in} \\ & V_{opmax} := V_{op} \left(\frac{\pi}{2} \right) \\ & V_{opmax} = 179.605 V \\ & V_{on}(\alpha) := \frac{D_n(\alpha)}{n \cdot (1 - D_n(\alpha))} \cdot V_{in} \\ & V_{onmax} := V_{on} \left(\frac{3\pi}{2} \right) \\ \end{split}$$

Corrente de Magnetização:

$$I_{Lmp}(\alpha) := \frac{I_o(\alpha)}{n \cdot (1 - D_p(\alpha))}$$

Ondulação de Corrente na Indutância de Magnetização:

$$\Delta I_{Lm}(\alpha) := \frac{D_p(\alpha) \cdot V_{in}}{f_s \cdot L_m}$$

$$\Delta I_{Lm_max} := \Delta I_{Lm}\left(\frac{\pi}{2}\right) \qquad \Delta I_{Lm_max} = 9.926 \text{ A}$$

Correntes nas Indutâncias de Magnetização:

$$\begin{split} \mathbf{I}_{\mathrm{Lmpl}}(\alpha) &\coloneqq \frac{2\mathbf{f}_{\mathrm{s}}\cdot\mathbf{L}_{\mathrm{m}}\cdot\mathbf{I}_{\mathrm{o}}(\alpha) - \mathbf{D}_{\mathrm{p}}(\alpha)\cdot(1 - \mathbf{D}_{\mathrm{p}}(\alpha))\cdot\mathbf{n}\cdot\mathbf{V}_{\mathrm{in}}}{2\mathbf{f}_{\mathrm{s}}\cdot\mathbf{L}_{\mathrm{m}}\cdot\mathbf{n}\cdot(1 - \mathbf{D}_{\mathrm{p}}(\alpha))} \\ \mathbf{I}_{\mathrm{Lmp2}}(\alpha) &\coloneqq \frac{2\mathbf{f}_{\mathrm{s}}\cdot\mathbf{L}_{\mathrm{m}}\cdot\mathbf{I}_{\mathrm{o}}(\alpha) + \mathbf{D}_{\mathrm{p}}(\alpha)\cdot(1 - \mathbf{D}_{\mathrm{p}}(\alpha))\cdot\mathbf{n}\cdot\mathbf{V}_{\mathrm{in}}}{2\mathbf{f}_{\mathrm{s}}\cdot\mathbf{L}_{\mathrm{m}}\cdot\mathbf{n}\cdot(1 - \mathbf{D}_{\mathrm{p}}(\alpha))} \\ \mathbf{I}_{\mathrm{Lmm1}}(\alpha) &\coloneqq -\frac{2\mathbf{f}_{\mathrm{s}}\cdot\mathbf{L}_{\mathrm{m}}\cdot\mathbf{I}_{\mathrm{o}}(\alpha) - \mathbf{D}_{\mathrm{n}}(\alpha)\cdot(1 - \mathbf{D}_{\mathrm{n}}(\alpha))\cdot\mathbf{n}\cdot\mathbf{V}_{\mathrm{in}}}{2\mathbf{f}_{\mathrm{s}}\cdot\mathbf{L}_{\mathrm{m}}\cdot\mathbf{n}\cdot(1 - \mathbf{D}_{\mathrm{n}}(\alpha))} \\ \\ 2\mathbf{f}_{\mathrm{s}}\cdot\mathbf{L}_{\mathrm{m}}\cdot\mathbf{n}\cdot(1 - \mathbf{D}_{\mathrm{n}}(\alpha)) \\ \end{split}$$

$$I_{Lmn2}(\alpha) := -\frac{2f_{s} \cdot L_{m} \cdot I_{o}(\alpha) + D_{n}(\alpha) \cdot (1 - D_{n}(\alpha)) \cdot n \cdot V_{in}}{2f_{s} \cdot L_{m} \cdot n \cdot (1 - D_{n}(\alpha))}$$

Valor Médio de Corrente nos Interruptores:

$$\begin{split} \mathbf{I}_{\mathrm{Splmed}} &:= \frac{1}{2\pi} \cdot \int_{0}^{\pi} \frac{(\mathbf{I}_{\mathrm{Lmpl}}(\alpha) + \mathbf{I}_{\mathrm{Lmp2}}(\alpha)) \cdot \mathbf{D}_{p}(\alpha)}{2} \, d\alpha & \mathbf{I}_{\mathrm{Splmed}} = 3.571 \, \mathrm{A} \\ \mathbf{I}_{\mathrm{Splmed}} &:= \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{(\mathbf{I}_{\mathrm{Lmpl}}(\alpha) + \mathbf{I}_{\mathrm{Lmp2}}(\alpha)) \cdot (1 - \mathbf{D}_{p}(\alpha))}{2} \, d\alpha & \mathbf{I}_{\mathrm{Splmed}} = 0 \, \mathrm{A} \\ \mathbf{I}_{\mathrm{Snlmed}} &:= \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{(\mathbf{I}_{\mathrm{Lmnl}}(\alpha) + \mathbf{I}_{\mathrm{Lmn2}}(\alpha)) \cdot \mathbf{D}_{n}(\alpha)}{2} \, d\alpha & \mathbf{I}_{\mathrm{Snlmed}} = 3.571 \, \mathrm{A} \\ \mathbf{I}_{\mathrm{Snlmed}} &:= \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{(\mathbf{I}_{\mathrm{Lmnl}}(\alpha) + \mathbf{I}_{\mathrm{Lmn2}}(\alpha)) \cdot \mathbf{D}_{n}(\alpha)}{2} \, d\alpha & \mathbf{I}_{\mathrm{Snlmed}} = 3.571 \, \mathrm{A} \\ \mathbf{I}_{\mathrm{Snlmed}} &:= \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{(\mathbf{I}_{\mathrm{Lmnl}}(\alpha) + \mathbf{I}_{\mathrm{Lmn2}}(\alpha)) \cdot (1 - \mathbf{D}_{n}(\alpha))}{2} \, d\alpha & \mathbf{I}_{\mathrm{Snlmed}} = 0 \, \mathrm{A} \end{split}$$

Valor Eficaz de Corrente nos Interruptores:

$$\mathbf{I_{Splef}} \coloneqq \sqrt{\frac{1}{2\pi}} \cdot \int_{0}^{2\pi} \frac{\left(\mathbf{I_{Lmpl}}(\alpha)^{2} + \mathbf{I_{Lmpl}}(\alpha) \cdot \mathbf{I_{Lmp2}}(\alpha) + \mathbf{I_{Lmp2}}(\alpha)^{2}\right) \cdot \mathbf{D_{p}}(\alpha)}{3} \, d\alpha$$

 $I_{Splef} = 7.548 A$

$$I_{\text{Sp2ef}} := \sqrt{\frac{n^2}{2\pi}} \cdot \int_0^{2\pi} \frac{\left(I_{\text{Lmp1}}(\alpha)^2 + I_{\text{Lmp1}}(\alpha) \cdot I_{\text{Lmp2}}(\alpha) + I_{\text{Lmp2}}(\alpha)^2\right) \cdot \left(1 - D_p(\alpha)\right)}{3} d\alpha$$

 $I_{Sp2ef} = 5.777 A$

$$I_{\text{Snlef}} \coloneqq \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} \frac{\left(I_{\text{Lmnl}}(\alpha)^{2} + I_{\text{Lmnl}}(\alpha) \cdot I_{\text{Lmn2}}(\alpha) + I_{\text{Lmn2}}(\alpha)^{2}\right) \cdot D_{n}(\alpha)}{3} \, d\alpha$$
$$I_{\text{Smlef}} = 7.548 \, \text{A}$$

$$I_{\text{Sn2ef}} := \sqrt{\frac{n^2}{2\pi}} \cdot \int_0^{2\pi} \frac{\left(I_{\text{Lmn1}}(\alpha)^2 + I_{\text{Lmn1}}(\alpha) \cdot I_{\text{Lmn2}}(\alpha) + I_{\text{Lmn2}}(\alpha)^2\right) \cdot \left(1 - D_n(\alpha)\right)}{3} d\alpha}$$
$$I_{\text{Sn2ef}} = 5.777 \text{ A}$$

Valor Eficaz de Corrente nos Enrolamentos dos Indutores Acoplados:

I _{Tplef} := I _{Splef}	$I_{Tplef} = 7.548 \text{A}$
I _{Tp2ef} := I _{Sp2ef}	$I_{Tp2ef} = 5.777 \text{A}$
I _{Tnlef} := I _{Snlef}	$I_{\texttt{Tnlef}} = 7.548\text{A}$
I _{Tn2ef} := I _{Sn2ef}	$I_{\text{Tn2ef}} = 5.777 \text{A}$

Valor Máximo de Corrente nas Indutâncias de Magnetização:

$I_{Lmpmax} := I_{Lmp2}\left(\frac{\pi}{2}\right)$	$I_{Lmpmax} = 24.817 A$
$I_{Lmnmax} := I_{Lmnl}\left(\frac{3\pi}{2}\right)$	$I_{Lmnmax} = 24.817 A$

Valor Máximo de Tensão nos Interruptores:

$$\begin{split} & V_{Sp1}(\boldsymbol{\omega}) \coloneqq V_{in} + n \cdot V_{op}(\boldsymbol{\omega}) \\ & V_{Sp1max} \coloneqq V_{Sp1} \left(\frac{\pi}{2} \right) & V_{Sp1max} \equiv 249.605 \, V \\ & V_{Sp2}(\boldsymbol{\omega}) \coloneqq \frac{V_{in}}{n} + V_{op}(\boldsymbol{\omega}) \\ & V_{Sp2max} \coloneqq V_{Sp2} \left(\frac{\pi}{2} \right) & V_{Sp2max} \equiv 249.605 \, V \\ & V_{Sn1}(\boldsymbol{\omega}) \coloneqq V_{in} + n \cdot V_{on}(\boldsymbol{\omega}) \\ & V_{Sn1max} \coloneqq V_{Sn1} \left(\frac{3\pi}{2} \right) & V_{Sn1max} \equiv 249.605 \, V \end{split}$$

$$\begin{split} & \mathrm{V}_{\mathrm{Sn2}}(\alpha) := \frac{\mathrm{V}_{\mathrm{in}}}{n} + \mathrm{V}_{\mathrm{on}}(\alpha) \\ & \mathrm{V}_{\mathrm{Sn2max}} := \mathrm{V}_{\mathrm{Sn2}}\!\!\left(\frac{3\pi}{2}\right) \end{split}$$

V_{Sn2max} = 249.605 V

Semicondutores Escolhidos:

Interruptores S1p, S2p, S1n e S2n: IKW40N65F5 (IGBT)

Cálculos de Perdas:

V_{THOIGBT} := 1.25V

 $R_{onIGBT} := 0.01\Omega$

V_{THOD} := 0.98V

 $R_{D.} := 0.022\Omega$

Para Rg = 15 Ω

$$\begin{split} \mathbf{k_{on1}} &\coloneqq 1.75 \cdot 10^{-5} \frac{J}{A} \\ \mathbf{k_{on2}} &\coloneqq 3.75 \cdot 10^{-7} \frac{J}{A^2} \\ \mathbf{k_{off1}} &\coloneqq 6.75 \cdot 10^{-6} \frac{J}{A} \\ \mathbf{k_{off2}} &\coloneqq 1.125 \cdot 10^{-7} \frac{J}{A^2} \\ \mathbf{V_{CEref}} &\coloneqq 400 \mathbf{V} \\ \mathbf{E_{on}}(\mathbf{I_C}, \mathbf{V_{CE}}) &\coloneqq \left(\mathbf{k_{on1}} \cdot \mathbf{I_C} + \mathbf{k_{on2}} \cdot \mathbf{I_C}^2\right) \cdot \frac{\mathbf{V_{CE}}}{\mathbf{V_{CEref}}} \\ \mathbf{E_{off}}(\mathbf{I_C}, \mathbf{V_{CE}}) &\coloneqq \left(\mathbf{k_{off1}} \cdot \mathbf{I_C} + \mathbf{k_{off2}} \cdot \mathbf{I_C}^2\right) \cdot \frac{\mathbf{V_{CE}}}{\mathbf{V_{CEref}}} \end{split}$$

$P_{\text{Splcond}} \coloneqq V_{\text{TH0IGBT}} I_{\text{Splmed}} + R_{\text{onIGBT}} I_{\text{Splef}}^2$	
$P_{Sp2cond} \coloneqq V_{TH0IGBT}I_{Sp2med} + R_{onIGBT}I_{Sp2ef}^{2}$	

 $P_{Splcond} = 5.034 W$ $P_{Sp2cond} = 0.334 W$

$P_{Snlcond} := V_{TH0IGBT}I_{Snlmed} + R_{onIGBT}I_{Snlef}^{2}$	$P_{Snlcond} = 5.034 W$
$P_{Sn2cond} := V_{TH0IGBT}I_{Sn2med} + R_{onIGBT}I_{Sn2ef}^{2}$	$P_{\rm Sn2cond} = 0.334\rm W$

P_{Scond} := P_{Splcond} + P_{Splcond} + P_{Snlcond} + P_{Snlcond}

 $P_{Scond} = 10.736 W$

$$E_{\text{Splcom}}(\alpha) := E_{\text{on}}(I_{\text{Lmpl}}(\alpha), V_{\text{Spl}}(\alpha)) + E_{\text{off}}(I_{\text{Lmp2}}(\alpha), V_{\text{Spl}}(\alpha))$$

$$P_{\text{Splcom}} \coloneqq \frac{f_5}{2\pi} \cdot \int_0^{\pi} E_{\text{Splcom}}(\alpha) \, d\alpha \qquad \qquad P_{\text{Splcom}} = 1.551 \, \text{W}$$

 $\mathbb{E}_{\text{Sp2com}}(\alpha) \coloneqq \mathbb{E}_{\text{on}}\left(n \left| I_{\text{Lmp1}}(\alpha) \right|, \mathbb{V}_{\text{Sp2}}(\alpha)\right) + \mathbb{E}_{\text{off}}\left(n \left| I_{\text{Lmp2}}(\alpha) \right|, \mathbb{V}_{\text{Sp2}}(\alpha)\right)$

$$P_{\text{Sp2com}} := \frac{f_{\text{s}}}{2\pi} \cdot \int_{\pi}^{2\pi} E_{\text{Sp2com}}(\alpha) \, d\alpha \qquad \qquad P_{\text{Sp2com}} = 0.164 \, \text{W}$$

 $\mathsf{E}_{\mathrm{Snl\,com}}(\alpha) := \mathsf{E}_{\mathrm{on}}(\mathsf{I}_{\mathrm{Lmn2}}(\alpha), \mathsf{V}_{\mathrm{Snl}}(\alpha)) + \mathsf{E}_{\mathrm{off}}(\mathsf{I}_{\mathrm{Lmn1}}(\alpha), \mathsf{V}_{\mathrm{Snl}}(\alpha))$

 $P_{\text{Snlcom}} := \frac{f_5}{2\pi} \cdot \int_{\pi}^{2\pi} E_{\text{Snlcom}}(\alpha) \, d\alpha \qquad \qquad P_{\text{Snlcom}} = 1.551 \, \text{W}$

 $\mathbf{E}_{\text{Sn2com}}(\alpha) := \mathbf{E}_{\text{on}}\left(n \left| \mathbf{I}_{\text{Lmn2}}(\alpha) \right|, \mathbf{V}_{\text{Sn2}}(\alpha)\right) + \mathbf{E}_{\text{off}}\left(n \left| \mathbf{I}_{\text{Lmn1}}(\alpha) \right|, \mathbf{V}_{\text{Sn2}}(\alpha)\right)$

$$\begin{split} P_{\text{Sn2com}} &\coloneqq \frac{f_{\text{s}}}{2\pi} \int_{0}^{\pi} E_{\text{Sn2com}}(\alpha) \, d\alpha & P_{\text{Sn2com}} = 0.164 \text{W} \\ P_{\text{Scom}} &\coloneqq P_{\text{Sp1com}} + P_{\text{Sp2com}} + P_{\text{Sn2com}} + P_{\text{Sn2com}} & P_{\text{Scom}} = 3.43 \text{W} \\ P_{\text{Stotal}} &\coloneqq P_{\text{Scom}} + P_{\text{Scom}} & P_{\text{Stotal}} = 14.166 \text{W} \\ R_{\text{cobrel}} &\coloneqq 86 \cdot 10^{-3} \cdot \Omega & P_{\text{Scohrel}} := 86 \cdot 10^{-3} \cdot \Omega & P_{\text{Scohrel}} := 110 \cdot 10^{-3} \cdot \Omega & P_{\text{Tpcohrel}} := R_{\text{cobrel}} \cdot I_{\text{Tplef}}^{2} + R_{\text{cobre2}} \cdot I_{\text{Tp2ef}}^{2} & P_{\text{Tpcohrel}} = 8.571 \text{W} \\ P_{\text{Tncohrel}} &\coloneqq R_{\text{cobrel}} \cdot I_{\text{Thlef}}^{2} + R_{\text{cobre2}} \cdot I_{\text{Tn2ef}}^{2} & P_{\text{Tncohrel}} = 8.571 \text{W} \end{split}$$

 $P_{\text{Ttotal}} \coloneqq P_{\text{Tpcond}} + P_{\text{Tncond}} + P_{\text{Tpmag}} + P_{\text{Tnmag}}$

$$\begin{split} & L_{d} := 4 \mu H \\ & \mathbb{P}_{clamp} := \frac{1}{2\pi} \cdot f_{5} \cdot L_{d} \cdot \int_{0}^{\pi} \mathbb{I}_{Lmp2}(\alpha)^{2} \, d\alpha \end{split}$$

Estimativa de Rendimento:

 $\eta \coloneqq \frac{P_o}{P_o + P_{Stotal} + P_{Ttotal} + 4P_{clamp}}$

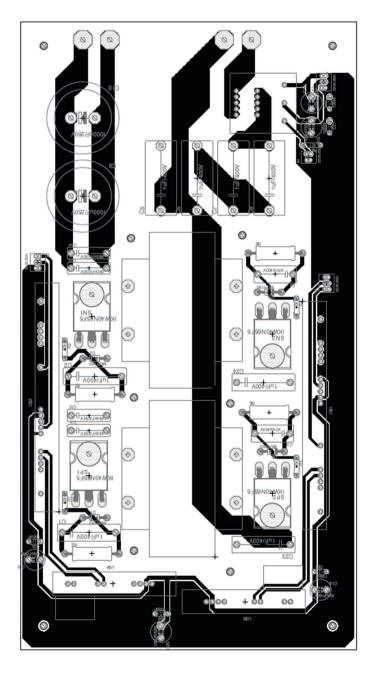
 $P_{Ttotal} = 20.01 \, W$

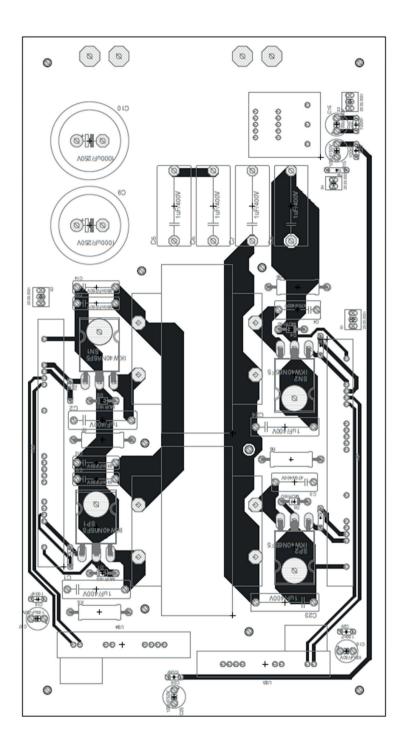
 $P_{elamp} = 11.001 W$

 $\eta = 86.478.\%$

APPENDIX F

APPENDIX F – DC-AC FLYBACK CONVERTER WITH DIFFERENTIAL OUTPUT CONNECTION – PCB LAYOUT





APPENDIX G

APPENDIX G – CALCULATIONS FOR THE ACTIVE-CLAMPING DC/AC FLYBACK CONVERTER – 100 KHZ

Active-clamping Flyback DC/AC Converter - 100 kHz

1. Specifications:

Input Voltage:	V _{IN} := 70V	
RMS Output Voltage:	$V_{ef} := 127V$	
Average Output Power:	P _o := 500W	
Switching Frequency:	$\mathbf{f}_{s} := 100 \mathrm{kHz}$	
Current Ripple in Lm:	$\Delta I_{Lm\%} := 30\%$	
Output Voltage Ripple:	ΔV _{0%} := 17%	
Auxiliary Switching Capacitor Voltage Ripple:	$\Delta V_{CG\%} := 5\%$	
AC Voltage Ripple:	ΔV _{%_AC} := 27.2%	
Switching Frequency Period:	$\mathbf{T}_{\mathrm{s}} := \frac{1}{f_{\mathrm{s}}}$	$T_s = 10 \cdot \mu s$
2. Design Requirements:		
2. Design Requirements: Modulation Index:		
2. Design Requirements: <u>Modulation Index:</u> M:= 0.6		
Modulation Index:		
Modulation Index: M := 0.6		
<u>Modulation Index:</u> M := 0.6 <u>Auxiliary Switching Inductor:</u>		
$\label{eq:Modulation Index:} \begin{split} \underline{\text{M}} &\coloneqq 0.6 \\ \\ \underline{\text{Auxiliary Switching Inductor:}} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ $		
$\label{eq:modulation_index:} \begin{split} \underline{M} &:= 0.6 \\ \\ \underline{Auxiliary Switching Inductor:} \\ \\ L_G &:= 2 \mu H \\ \\ \hline \textbf{3. Preliminary Calculations:} \end{split}$	V _o = 179.605 V	
$\label{eq:modulation_index:} \begin{split} \underline{M} &:= 0.6 \\ \\ \underline{Auxiliary Switching Inductor:} \\ \\ L_G &:= 2 \mu H \\ \\ \hline \begin{array}{c} \textbf{3. Preliminary Calculations:} \\ \\ \underline{Average Peak Voltage:} \\ \end{array} \end{split}$	V _o = 179.605 V	
$\label{eq:modulation_index:} \begin{split} \underline{M} &:= 0.6 \\ \\ \underline{Auxiliary Switching Inductor:} \\ L_G &:= 2 \mu H \\ \\ \hline \textbf{3. Preliminary Calculations:} \\ \\ \underline{Average Peak Voltage:} \\ V_o &:= \sqrt{2} \cdot V_{ef} \end{split}$	V _o = 179.605 V I _{o_max} = 5.568 A	
$\label{eq:modulation Index:} \hline M \coloneqq 0.6 \\ \hline M \coloneqq 0.6 \\ \hline Auxiliary Switching Inductor: \\ L_G \coloneqq 2 \mu H \\ \hline \textbf{3. Preliminary Calculations:} \\ \hline Average Peak Voltage: \\ V_o \coloneqq \sqrt{2} \cdot V_{ef} \\ \hline Output Current: \\ \hline \end{array}$		

Load Resistance:

 $R_o := \frac{V_o}{I_o_max}$

 $R_0 = 32.258 \Omega$

Flyback Inductor Turns Ratio:	
$n := \frac{v_o}{M \cdot V_{IN}}$	n = 4.276
Vo/n Relation:	
$V_o := \frac{V_o}{n}$	V_o = 42 V
Alternate Output Voltage:	
$V_{o_AC}(\alpha) \coloneqq V_{o} \cdot \sin(\alpha)$	$V_{o_AC}\left(\frac{\pi}{2}\right) = 179.605 V$
Paarameterizid Output Current:	

$$\mathbf{I_{o_barra}}(\alpha) := \frac{2 \cdot \mathbf{f_s} \cdot \mathbf{L_{G^*}n}}{V_{\mathrm{IN}}} \cdot \mathbf{I_o}(\alpha) \qquad \qquad \mathbf{I_{o_barra}}\left(\frac{\pi}{2}\right) = 0.136$$

Duty Cycle and Inductance Factor:

$$\begin{split} \mathbf{D} &:= 0.5 \qquad \lambda := 0.1 \\ & \text{Given} \\ & \mathbf{I}_{0_\text{barra}}\!\!\left(\frac{\pi}{2}\right) = \frac{\mathbf{D} + \mathbf{D}\cdot\lambda\cdot\mathbf{M} + \mathbf{D}\cdot\mathbf{M} - \mathbf{M}\cdot(\lambda+1)}{1 + \mathbf{M}\cdot\lambda + \mathbf{M}} \\ & \Delta\mathbf{I}_{\text{Lm}\%} = \frac{2\cdot\lambda\cdot\mathbf{M}}{(\mathbf{M}+1)\cdot(\mathbf{D}-\mathbf{M}+\mathbf{D}\cdot\mathbf{M}-\lambda\cdot\mathbf{M}+\mathbf{D}\cdot\lambda\cdot\mathbf{M})} \\ & \text{sol} := \text{Minerr}(\mathbf{D},\lambda) \\ & \mathbf{D}_{w} := \text{sol}_{0} \qquad \qquad \mathbf{D} = 0.531 \\ & \mathbf{\lambda} := \text{sol}_{1} \qquad \qquad \mathbf{\lambda} = 0.09 \end{split}$$

Duty Cycle for S1 e SG:

 $q(\alpha) := M \cdot \sin(\alpha)$

$$\begin{split} \mathsf{D}_{\mathrm{ac}}(\alpha) &\coloneqq \begin{array}{c} \mathsf{I}_{0_\mathrm{barra}}(\alpha) \cdot (q(\alpha) \cdot \lambda + q(\alpha) + 1) + q(\alpha) \cdot (\lambda + 1) \\ q(\alpha) \cdot \lambda + q(\alpha) + 1 & \text{if } 0 < \alpha < \pi \\ \hline -\mathsf{I}_{0_\mathrm{barra}}(\alpha) \cdot (-q(\alpha) \cdot \lambda - q(\alpha) + 1) - q(\alpha) \cdot (\lambda + 1) \\ \hline -q(\alpha) \cdot \lambda - q(\alpha) + 1 & \text{otherwise} \end{array} \quad \begin{array}{c} \mathsf{D}_{\mathrm{ac}}\left(\frac{\pi}{2}\right) = 0.531 \\ \hline \mathsf{D}_{\mathrm{ac}}\left(\frac{3\pi}{2}\right) = 0.531 \end{split}$$

Duty Cycle for SP e DP:

$$\begin{split} \mathbf{D}_{ac_SP}(\alpha) &:= \begin{array}{|c|c|} \frac{\mathbf{I}_{o_barra}(\alpha) \cdot (q(\alpha) \cdot \lambda + q(\alpha) + 1) + q(\alpha) \cdot (\lambda + 1)}{q(\alpha) \cdot \lambda + q(\alpha) + 1} & \text{if } 0 < \alpha < \pi \\ \hline \mathbf{D}_{ac_SP}\left(\frac{\pi}{2}\right) = 0.531 \\ \hline \mathbf{D}_{ac_SP}\left(\frac{3\pi}{2}\right) = 0 \end{split}$$

Duty Cycle for SN e DN:

$$\begin{split} \mathbf{D}_{ac_SN}(\alpha) &\coloneqq & \begin{array}{c} 0 \quad \text{if } 0 < \alpha < \pi \\ & \frac{-\mathbf{I}_{o_barra}(\alpha) \cdot (-q(\alpha) \cdot \lambda - q(\alpha) + 1) - q(\alpha) \cdot (\lambda + 1)}{-q(\alpha) \cdot \lambda - q(\alpha) + 1} & \begin{array}{c} \mathbf{D}_{ac_SN}(\alpha) \\ & \mathbf{D}_{ac_SN}(\alpha) \\ & \begin{array}{c} \mathbf{D}_{ac_SN}(\alpha) \\ & \end{array} \\ & \begin{array}{c} \mathbf{D}_{ac_SN}(\alpha) \\ & \begin{array}{c} \mathbf{D}_{ac_SN}(\alpha) \\ & \end{array} \\ & \begin{array}{c} \mathbf{D}_{ac_SN}(\alpha) \\ & \end{array} \\ & \begin{array}{c} \mathbf{D}_{ac_SN}(\alpha) \\ & \end{array} \\ & \end{array} \end{array} \end{array} \end{array}$$

$$D_{ac_SN}\left(\frac{\pi}{2}\right) = 0$$
$$D_{ac_SN}\left(\frac{3\pi}{2}\right) = 0.531$$

Magnetizing Inductance Lm:

$$L_{M} := \frac{L_{G}}{\lambda}$$

$$L_{M} = 22.219 \cdot \mu H$$

V_{CG} = -79.401 V

Voltage on Auxiliary Switching Capacitor Cg:

$$V_{CG} \coloneqq \frac{D \cdot V_{IN}}{-1 + D}$$

Minimum Current in Lm:

$$I_{1} := \frac{\lambda \cdot \left[V_{IN} \cdot V_{-} \circ (D-2) + V_{-} \circ^{2} \cdot (D-1) \right] + D \left(V_{IN} + V_{-} \circ \right)^{2} - V_{-} \circ \left(V_{IN} + V_{-} \circ \right)}{2\lambda \cdot f_{5} \cdot \left[V_{-} \circ L_{G} + L_{M} \left(V_{IN} + V_{-} \circ \right) \right]}$$

 $I_1 = 32.381 \text{ A}$

Minimum Current in Lm (AC):

$$\begin{split} & \mathbb{A}_{LM01}(\alpha) \coloneqq \mathbb{V}_{IN} \cdot \frac{\mathbb{V}_{o_AC}(\alpha)}{n} \cdot \left(\mathbb{D}_{ac}(\alpha) - 2 \right) + \left(\frac{\mathbb{V}_{o_AC}(\alpha)}{n} \right)^2 \cdot \left(\mathbb{D}_{ac}(\alpha) - 1 \right) \\ & \mathbb{A}_{LM02}(\alpha) \coloneqq \mathbb{V}_{IN} \cdot \frac{-\mathbb{V}_{o_AC}(\alpha)}{n} \cdot \left(\mathbb{D}_{ac}(\alpha) - 2 \right) + \left(\frac{-\mathbb{V}_{o_AC}(\alpha)}{n} \right)^2 \cdot \left(\mathbb{D}_{ac}(\alpha) - 1 \right) \end{split}$$

$$\begin{split} \mathbf{I}_{1_AC}(\alpha) \coloneqq & \left[\begin{array}{c} \frac{\lambda \cdot \left(A_{\underline{\mathrm{LM01}}}(\alpha) \right) + \mathbf{D}_{ac}(\alpha) \cdot \left(\mathbf{V}_{\underline{\mathrm{IN}}} + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right)^2 - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \cdot \left(\mathbf{V}_{\underline{\mathrm{IN}}} + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right)}{n} & \text{if } 0 < \alpha < \pi \\ \\ & \frac{2\lambda \cdot \mathbf{f}_5 \left[\frac{\mathbf{V}_{0_AC}(\alpha)}{n} \cdot \mathbf{L}_G + \mathbf{L}_M \left(\mathbf{V}_{\underline{\mathrm{IN}}} + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right) \right]}{1} & \text{otherwise} \\ & \frac{\lambda \cdot \left(A_{\underline{\mathrm{LM02}}}(\alpha) \right) + \mathbf{D}_{ac}(\alpha) \cdot \left(\mathbf{V}_{\underline{\mathrm{IN}}} - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right)^2 + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \cdot \left(\mathbf{V}_{\underline{\mathrm{IN}}} - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right)}{n} & \text{otherwise} \\ & \frac{2\lambda \cdot \mathbf{f}_5 \left[-\frac{-\mathbf{V}_{0_AC}(\alpha)}{n} \cdot \mathbf{L}_G + \mathbf{L}_M \left(\mathbf{V}_{\underline{\mathrm{IN}}} - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right) \right]}{11_AC\left(\frac{\pi}{2} \right) = 32.381 \, \mathrm{A}} \\ & \mathbf{I}_{1_AC}\left(\frac{3\pi}{2} \right) = 32.381 \, \mathrm{A} \end{split}$$

Máximum Current in Lm:

$$I_{2} := \frac{1}{2} \frac{V_{IN} D + D V_{o} - V_{o}}{L_{G} f_{s}}$$

$$I_{2} = 43.81 \text{ A}$$

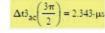
Maximum Current in Lm (AC):

$$\begin{split} \mathbf{I}_{2_AC}(\alpha) &\coloneqq \begin{bmatrix} \frac{1}{2} \cdot \frac{\mathbf{V}_{\mathbb{I}\mathbb{N}} \cdot \mathbf{D}_{ac}(\alpha) + \mathbf{D}_{ac}(\alpha) \cdot \frac{\mathbf{V}_{0_AC}(\alpha)}{n} - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \\ \frac{1}{2} \cdot \frac{\mathbf{V}_{\mathbb{I}\mathbb{N}} \cdot \mathbf{D}_{ac}(\alpha) + \mathbf{D}_{ac}(\alpha) \cdot \frac{-\mathbf{V}_{0_AC}(\alpha)}{n} + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \\ \frac{1}{2} \cdot \frac{\mathbf{V}_{\mathbb{I}\mathbb{N}} \cdot \mathbf{D}_{ac}(\alpha) + \mathbf{D}_{ac}(\alpha) \cdot \frac{-\mathbf{V}_{0_AC}(\alpha)}{n} + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \\ \mathbf{I}_{G^{*}} \mathbf{f}_{5} \end{bmatrix} \text{ otherwise} \\ \begin{bmatrix} \mathbf{I}_{2_AC}\left(\frac{\pi}{2}\right) = 43.81 \, \mathrm{A} \\ \mathbf{I}_{2_AC}\left(\frac{3\pi}{2}\right) = 43.81 \, \mathrm{A} \end{bmatrix} \end{split}$$

4. Operating Stages Duration:

1st Operating Stage (I1->I2): $\Delta t l := \frac{(I_2 - I_1) \cdot (L_G + L_M)}{V_{DM}}$ $\Delta t1 = 3.954 \, \mu s$ 1st Operating Stage (AC): $\Delta tl_{ac}(\alpha) := \frac{\left(I_2 AC(\alpha) - I_1 AC(\alpha)\right) \cdot \left(L_G + L_M\right)}{V_{DJ}}$ $\Delta t l_{ac} \left(\frac{\pi}{2} \right) = 3.954 \, \mu s$ 3rd Operating Stage (12->0): $\Delta t3 := \frac{(1-D)}{2 \cdot f_{\star}}$ Δt^3 3rd Operating Stage (AC): $\Delta t \beta_{ac}(\alpha) := \frac{\left(1 - D_{ac}(\alpha)\right)}{2 \cdot f}$ 4th Operating Stage (0-> -12): $\Delta t4 := \Delta t3$ $\Delta t4 = 2.343 \, \mu s$ 4th Operating Stage (AC): $\Delta t4_{ac}(\alpha) := \Delta t3_{ac}(\alpha)$

6th Operating Stage (-I2->0): $\Delta t6 := \frac{V_{IN} \cdot D + D \cdot V_o - V_o}{2(V_{IN} + V_o) \cdot f_s}$





 $\Delta t6 = 0.782 \cdot \mu s$

6th Operating Stage (AC):

$$\begin{split} \Delta t 6_{ac}(\alpha) &\coloneqq \left(\begin{array}{c} \frac{V_{\underline{I}N} D_{ac}(\alpha) + D_{ac}(\alpha) \cdot \frac{V_{\underline{0}_AC}(\alpha)}{n} - \frac{V_{\underline{0}_AC}(\alpha)}{n}}{2 \left(V_{\underline{I}N} + \frac{V_{\underline{0}_AC}(\alpha)}{n} \right) \cdot \mathbf{f}_{5}} & \text{if } 0 < \alpha < \pi \\ \\ \frac{V_{\underline{I}N} D_{ac}(\alpha) - D_{ac}(\alpha) \cdot \frac{V_{\underline{0}_AC}(\alpha)}{n} + \frac{V_{\underline{0}_AC}(\alpha)}{n}}{2 \left(V_{\underline{I}N} - \frac{V_{\underline{0}_AC}(\alpha)}{n} \right) \cdot \mathbf{f}_{5}} & \text{otherwise} \\ \\ \frac{\Delta t 6_{ac} \left(\frac{3\pi}{2} \right) = 0.782 \cdot \mu s}{\Delta t 6_{ac} \left(\frac{3\pi}{2} \right) = 0.782 \cdot \mu s} \end{split}$$

7th Operating Stage (0->11):

$$\Delta t7 := \frac{L_G I_I}{V_{IN} + V_{-0}} \qquad \Delta t7 = 0.578 \cdot \mu s$$

Citizes Eters - Calida Alt

Sétima Etapa - Saída Alternada:

$$\Delta t \overline{\gamma}_{ac}(\alpha) := \frac{\frac{L_{G} I_{\underline{1}}\underline{AC}(\alpha)}{V_{\underline{IN}} + \frac{V_{\underline{0}}\underline{AC}(\alpha)}{n}} \text{ if } 0 < \alpha < \pi}{\frac{L_{G} I_{\underline{1}}\underline{AC}(\alpha)}{V_{\underline{IN}} - \frac{V_{\underline{0}}\underline{AC}(\alpha)}{n}}} \text{ otherwise}} \Delta t \overline{\gamma}_{ac}\left(\frac{\pi}{2}\right) = 0.578 \cdot \mu s$$

5. Intermediate Equations:

Lm current in ∆t6

$$I_{x} := \frac{I_{1} \cdot (\Delta t3 + \Delta t4) + I_{2} \cdot (\Delta t6 + \Delta t7)}{\Delta t3 + \Delta t4 + \Delta t6 + \Delta t7}$$
$$I_{x} = 34.953 \text{ A}$$

Lm current in Δt6 (AC)

$$\begin{split} I_{x_AC}(\alpha) &:= \frac{I_{1_AC}(\alpha) \cdot \left(\Delta t_{3ac}(\alpha) + \Delta t_{4ac}(\alpha)\right) + I_{2_AC}(\alpha) \cdot \left(\Delta t_{6ac}(\alpha) + \Delta t_{7ac}(\alpha)\right)}{\Delta t_{3ac}(\alpha) + \Delta t_{4ac}(\alpha) + \Delta t_{6ac}(\alpha) + \Delta t_{7ac}(\alpha)} \\ I_{x_AC}\left(\frac{\pi}{2}\right) &= 34.953 \text{ A} \end{split}$$

$$I_{x_AC}\left(\frac{3\pi}{2}\right) &= 34.953 \text{ A} \end{split}$$

Output Current Validation

$$\begin{split} I_{o_calc} &:= \frac{\left(I_2 + I_x\right) \cdot \mathbf{f}_{s} \cdot (\Delta t3 + \Delta t4)}{2 \cdot n} + \frac{\left(I_2 + I_x\right) \cdot \mathbf{f}_{s} \cdot (\Delta t6 + \Delta t7)}{2 \cdot n} \\ I_{o_calc} &= 5.568 \, \text{A} \end{split}$$

6. Auxiliary Switching Inductance Lg:

Average Current (DC) - Lg:

$$I_{LG} \coloneqq \frac{1}{T_s} \cdot \left[\int_0^{\Delta t1} \left[\frac{(I_2 - I_1) \cdot t}{\Delta t1} + I_1 \right] dt + \int_0^{\Delta t3 + \Delta t4} \left[\frac{(-2I_2) \cdot t}{(\Delta t3 + \Delta t4)} + I_2 \right] dt + \int_0^{\Delta t6 + \Delta t7} \left[\frac{(I_1 + I_2) \cdot t}{(\Delta t7 + \Delta t6)} - I_2 \right] dt \right]$$

$$I_{LG} = 14.286 \text{ A}$$

RMS Current (DC) - Lq:

$$I_{LG_rms} := \sqrt{\frac{1}{T_s}} \left[\int_0^{\Delta t1} \left[\frac{(I_2 - I_1) \cdot t}{\Delta t1} + I_1 \right]^2 dt + \int_0^{\Delta t3 + \Delta t4} \left[\frac{(-2I_2) \cdot t}{(\Delta t3 + \Delta t4)} + I_2 \right]^2 dt + \int_0^{\Delta t6 + \Delta t7} \left[\frac{(I_1 + I_2) \cdot t}{(\Delta t7 + \Delta t6)} - I_2 \right]^2 dt \right]$$

$$I_{LG_rms} = 30.792 \text{ A}$$

$$\frac{\text{Average Current (AC) - Lg:}}{I_{LG_AC} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{1_AC}(\alpha) + I_{2_AC}(\alpha)\right) \cdot \Delta t I_{ac}(\alpha) + \left(I_{1_AC}(\alpha) - I_{2_AC}(\alpha)\right) \cdot \left(\Delta t 6_{ac}(\alpha) + \Delta t 7_{ac}(\alpha)\right)}{2 \cdot T_{5}} d\alpha$$

$$I_{LG_AC} = 7.143 \text{ A}$$

RMS Current (AC) - Lq:

$$\begin{split} &A_{LG01}(\alpha) \coloneqq \left(I_{1_AC}(\alpha)^2 + I_{1_AC}(\alpha) \cdot I_{2_AC}(\alpha) + I_{2_AC}(\alpha)^2\right) \cdot \Delta t I_{ac}(\alpha) \\ &A_{LG02}(\alpha) \coloneqq \left(I_{2_AC}(\alpha)^2\right) \cdot \left(\Delta t \cdot I_{ac}(\alpha) + \Delta t \cdot I_{ac}(\alpha)\right) \\ &A_{LG03}(\alpha) \coloneqq \left(I_{1_AC}(\alpha)^2 - I_{1_AC}(\alpha) \cdot I_{2_AC}(\alpha) + I_{2_AC}(\alpha)^2\right) \cdot \left(\Delta t \cdot 6_{ac}(\alpha) + \Delta t \cdot 7_{ac}(\alpha)\right) \\ &I_{LG_AC_rms} \coloneqq \sqrt{\frac{1}{2\pi} \cdot \int_{0}^{2\pi} \left(\frac{A_{LG01}(\alpha) + A_{LG02}(\alpha) + A_{LG03}(\alpha)}{3 \cdot T_5}\right) d\alpha} \\ &I_{LG_AC_rms} = 20.452 \text{ A} \end{split}$$

Maximum Voltage on Lg:

$$V_{LG_{max}} = V_{IN} + \frac{V_{o_{a}AC}\left(\frac{\pi}{2}\right)}{n}$$
$$V_{LG_{max}} = 112 V$$

7. Magnetizing Inductance Lm:

Average Lm Current (DC):

$$I_{LM} := \frac{I_1 + I_2}{2}$$

$$I_{LM} := \frac{(I_2 - I_1) \cdot 2}{I_1 + I_2}$$

$$delta_I_{LM} := \frac{(I_2 - I_1) \cdot 2}{I_1 + I_2}$$

$$delta_I_{LM} = 0.3$$

Average Lm Current (AC):

$$I_{LM_AC} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{1_AC}(\alpha) + I_{2_AC}(\alpha)\right)}{2} d\alpha \qquad \qquad I_{LM_AC} = 22.3 \text{ A}$$

Average Lm Current (AC):

$$I_{LM_AC_RMS} \coloneqq \left\{ \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \left[\frac{(I_{1_AC}(\alpha) + I_{2_AC}(\alpha))}{2} \right]^2 d\alpha \quad I_{LM_AC_RMS} = 25.469 \text{ A} \right\}$$

Maximum voltage on Lm:

$$V_{LM_max} := V_{IN} - \frac{L_G V_{IN}}{L_G + L_M} \qquad \qquad V_{LM_max} = 64.219 V$$

8. Auxiliary Switching Capacitor - Cg:

Desired Voltage Ripple:

$$\Delta V_{CG} := V_{CG} \Delta V_{CG\%}$$

 $\Delta V_{CG} = -3.97 \cdot V$

Capacitance:

$$C_{\mathbf{G}} := \frac{-I_2 \cdot \Delta t3}{2 \cdot \Delta V_{\mathbf{CG}}}$$

$$C_{\mathbf{G}} = 12.926 \cdot \mu \mathbf{F}$$

Average Current (DC) - Cq:

$$\begin{split} I_{CG} &\coloneqq \frac{1}{T_s} \cdot \int_0^{\Delta t 3 + \Delta t 4} \left[\frac{(I_2 + I_2) \cdot t}{\Delta t^3 + \Delta t 4} - I_2 \right] dt \\ I_{CG} &= 0 \text{ A} \end{split}$$

RMS Current (DC) - Cq:

$$\begin{split} \mathbf{I}_{\mathbf{CG_mms}} &\coloneqq \sqrt{\frac{1}{\mathbf{T}_{s}}} \cdot \int_{0}^{\Delta t \mathbf{3} + \Delta t \mathbf{4}} \left[\frac{(\mathbf{I}_{2} + \mathbf{I}_{2}) \cdot t}{(\Delta t \mathbf{3} + \Delta t \mathbf{4} - \mathbf{I}_{2})^{2}} dt \\ \mathbf{I}_{\mathbf{CG_mms}} &= 17.313 \text{ A} \end{split}$$

Average Current (AC) - Cq:

$$\begin{split} I_{CG_AC} &\coloneqq \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \left[\frac{-I_{2_AC}(\alpha) \cdot \left(\Delta t \beta_{ac}(\alpha) - \Delta t 4_{ac}(\alpha) \right)}{2T_{s}} \right] d\alpha \\ I_{CG_AC} &= 0 \text{ A} \end{split}$$

RMS Current (AC) - Cq:

$$I_{CG_AC_RMS} := \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} \left[\frac{I_{2_AC}(\alpha)^2 \cdot \left(\Delta t^3_{ac}(\alpha) + \Delta t 4_{ac}(\alpha) \right)}{3T_s} \right] d\alpha$$
$$I_{CG_AC_RMS} = 12.447 \text{ A}$$

9. Main Switch - S1:

Average Current (DC) - S1:

 $I_{S1} := I_{CG} + I_{LG}$

$$I_{S1} = 14.286 \, \text{A}$$

RMS Current (DC) - S1:

$$I_{\text{S1_rms}} \coloneqq \sqrt{\frac{1}{T_s}} \left[\int_0^{\Delta t1} \left[\frac{(I_2 - I_1) \cdot t}{\Delta t_1} + I_1 \right]^2 dt + \int_0^{\Delta t6 + \Delta t7} \left[\frac{(I_2 + I_1) \cdot t}{\Delta t6 + \Delta t7} - I_2 \right]^2 dt \right]$$
$$I_{\text{S1_rms}} = 25.464 \text{ A}$$

Average Current (AC) - S1:

$$I_{S1_AC} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{(I_{1_AC}(\alpha) + I_{2_AC}(\alpha)) \cdot \Delta t I_{ac}(\alpha) + (I_{1_AC}(\alpha) - I_{2_AC}(\alpha)) \cdot (\Delta t \delta_{ac}(\alpha) + \Delta t 7_{ac}(\alpha))}{2 \cdot T_{s}} d\alpha$$

$$I_{S1_AC} = 7.143 \text{ A}$$

RMS Current (AC) - S1:

$$I_{S1_AC_RMS} \coloneqq \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} \frac{\left(I_{1_AC}(\alpha) + I_{2_AC}(\alpha)\right)^{2} \cdot \Delta t I_{ac}(\alpha) + \left(I_{1_AC}(\alpha) - I_{2_AC}(\alpha)\right)^{2} \cdot \left(\Delta t 6_{ac}(\alpha) + \Delta t 7_{ac}(\alpha)\right)}{3 \cdot T_{s}} d\alpha$$

$$I_{S1_AC_RMS} \equiv 17.723 \text{ A}$$

$$Maximum Voltage = S1:$$

 $V_{S1_{max}} := V_{IN} - V_{CG}$

10. Auxiliary Switch - Sg:

Average Current (DC) - Sq:

I_{SG} := I_{CG}

 $I_{SG} = 0A$

RMS Current (DC) - Sq:

 $I_{SG_{max}} := I_{CG_{max}}$

I_{SG_11115} = 17.313 A

Average Current (AC) - Sq:

 $I_{SG_AC} := I_{CG_AC}$

 $I_{SG_AC} = 0 A$

RMS Current (AC) - Sq:

ISG_AC_RMS := ICG_AC_RMS

 $I_{SG_{AC_{RMS}}} = 12.447 \text{ A}$

Maximum Voltage - SG:

 $V_{SG_{max}} := V_{S1_{max}}$

V_{SG_max} = 149.401 V

11. Output Filter Capacitor Co:

Desired Voltage Ripple:

 $\Delta V_o := V_o \cdot \Delta V_{o\%}$ $\Delta V_o = 30.533 \cdot V$

Capacitance:

$$C_o := \frac{I_o_{max} \cdot D}{\Delta V_o \cdot f_s}$$

 $C_o = 0.969 \cdot \mu F$

12. Blocking Diode DP:

 $I_{DP} := I_{o_calc}$ $I_{DP} = 5.568 A$ RMS Current (DC) - Dp:

$$I_{DP_rms} := \sqrt{\frac{1}{T_s}} \left[\int_0^{\Delta t3 + \Delta t4} \left[\frac{\left[\frac{I_2}{n} + \frac{I_x}{n}\right] \cdot t}{\Delta t3 + \Delta t4} \right]^2 dt + \int_0^{\Delta t6 + \Delta t7} \left[\frac{\left[\frac{-I_2}{n} - \frac{I_x}{n}\right] \cdot t}{\Delta t6 + \Delta t7} + \frac{I_2}{n} + \frac{I_x}{n} \right]^2 dt \right]$$

$$I_{DP_rms} = \$.268 A$$

Average Current (AC) - Dp:

$$I_{DP_AC} := \frac{1}{2\pi} \cdot \int_{0}^{\pi} \frac{(I_{x_AC}(\alpha) + I_{2_AC}(\alpha)) \cdot (\Delta t \beta_{ac}(\alpha) + \Delta t 4_{ac}(\alpha) + \Delta t 6_{ac}(\alpha) + \Delta t 7_{ac}(\alpha))}{2T_{s} \cdot n} d\alpha$$
$$I_{DP_AC} = 1.772 A$$

RMS Current (AC) - Dp:

$$I_{DP_AC_RMS} \coloneqq \sqrt{\frac{1}{2\pi}} \int_{0}^{\pi} \frac{\left(I_{x_AC}(\alpha) + I_{2_AC}(\alpha)\right)^{2} \cdot \left(\Delta t_{ac}^{3}(\alpha) + \Delta t_{ac}^{4}(\alpha) + \Delta t_{ac}^{6}(\alpha) + \Delta t_{ac}^{7}(\alpha)\right)}{3T_{s} \cdot n^{2}} d\alpha$$
$$I_{DP_AC_RMS} = 4.009 \text{ A}$$

Maximum Voltage - Dp:

$$V_{DP_max} := V_{o_AC} \left(\frac{\pi}{2}\right) + V_{o_AC} \left(\frac{\pi}{2}\right) \Delta V_{o\%} + V_{LM_max'} n$$
$$V_{DP_max} = 484.76 V$$

13. Blocking Diode DN:

Average Current (DC) - Dn:

I_{DN} := 0A

 $I_{DN} = 0$

RMS Current (DC) - Dn:

I_{DN_ms} := 0A

$$I_{DN_{ms}} = 0$$

Average Current (AC) - Dn:

$$I_{DN_AC} := \frac{1}{2\pi} \cdot \int_{\pi}^{2\pi} \frac{\left(I_{x_AC}(\alpha) + I_{2_AC}(\alpha)\right) \cdot \left(\Delta t \beta_{ac}(\alpha) + \Delta t 4_{ac}(\alpha) + \Delta t 6_{ac}(\alpha) + \Delta t 7_{ac}(\alpha)\right)}{2T_{s} \cdot n} d\alpha$$

$$I_{DN_AC} = 1.772 A$$

RMS Current (AC) - Dn:

$$I_{\text{DN_AC_RMS}} := \sqrt{\frac{1}{2\pi}} \int_{\pi}^{2\pi} \frac{\left(I_{\text{x_AC}}(\alpha) + I_{2_AC}(\alpha)\right)^2 \cdot \left(\Delta t_{ac}^3(\alpha) + \Delta t_{ac}^4(\alpha) + \Delta t_{ac}^6(\alpha) + \Delta t_{ac}^7(\alpha)\right)}{3T_5 \cdot n^2} \, d\alpha$$
$$I_{\text{DN_AC_RMS}} = 4.009 \, \text{A}$$

Maximum Voltage - Dn:

 $V_{\text{DN_max}} := -V_{o_AC} \left(\frac{3\pi}{2}\right) - V_{o_AC} \left(\frac{3\pi}{2}\right) \Delta V_{o\%} + V_{\text{LM_max}} \cdot n$ $V_{\text{DN_max}} = 484.76 \text{ V}$

14. Switch SP:

Average Current (DC) Sp:

 $I_{SP} := I_{o_calc}$

I_{SP} = 5.568 A

RMS Current (DC) - Sp:

I_{SP_rms} := I_{DP_rms}

I_{SP mms} = 8.268 A

Average Current (AC) - Sp:

 $I_{SP_AC} := I_{DP_AC}$

I_{SP AC} = 1.772 A

RMS Current (AC) - Sp:

 $I_{SP_AC_RMS} := I_{DP_AC_RMS}$

 $I_{SP_AC_RMS} = 4.009 A$

APPENDIX H

APPENDIX H - CALCULATIONS FOR THE ACTIVE-CLAMPING DC/AC FLYBACK CONVERTER – 50 KHZ

Active-clamping Flyback DC/AC Converter - 50 kHz

1. Specifications:

Input Voltage:	$V_{IIN} := 70V$	
RMS Output Voltage:	V _{ef} := 127V	
Average Output Power:	P _o := 500W	
Switching Frequency:	$\mathbf{f}_{s} := 50 \mathrm{kHz}$	
Current Ripple in Lm:	ΔI _{Lm%} := 50%	
Output Voltage Ripple:	$\Delta V_{0\%} := 17\%$	
Auxiliary Switching Capacitor Voltage Ripple:	$\Delta V_{CG\%} := 65\%$	
AC Voltage Ripple:	ΔV _{%_AC} := 27.2%	
Switching Frequency Period:	$T_s := \frac{1}{f_s}$	$T_s = 20 \cdot \mu s$
2. Design Requirements:		
Modulation Index:		
M := 0.6		
Auxiliary Switching Inductor:		
$L_G := 4 \mu H$		
3. Preliminary Calculations:		
Average Peak Voltage:		
$V_o := \sqrt{2} \cdot V_{ef}$	V _o = 179.605 V	
Output Current:		
$I_{o_max} := \frac{2 \cdot P_o}{V_o}$	I _{0_max} = 5.568 A	
$I_{0}(\alpha) \coloneqq I_{0_\max} \cdot \sin(\alpha)$		

Load Resistance:

$$R_o := \frac{V_o}{I_o_{max}}$$

 $R_0 = 32.258 \Omega$

Flyback Inductor Turns Ratio:	
$n := \frac{V_o}{M \cdot V_{IN}}$	n = 4.276
Vo/n Relation:	
$V_o := \frac{v_o}{n}$	V_o = 42 V
Alternate Output Voltage:	
$V_{o_AC}(\alpha) \coloneqq V_o \cdot \sin(\alpha)$	$V_{o_AC}\left(\frac{\pi}{2}\right) = 179.$

Paarameterizid Output Current:

$$I_{o_bana}(\alpha) := \frac{2 \cdot f_{5} \cdot L_{G'} n}{V_{IN}} \cdot I_{o}(\alpha)$$

$$I_{o_barra}\left(\frac{\pi}{2}\right) = 0.136$$

.605 V

Duty Cycle and Inductance Factor:

$$\begin{split} \mathbf{D} &:= 0.5 \qquad \lambda := 0.1 \\ & \text{Given} \\ & \mathbf{I}_{0_barra}\!\!\left(\frac{\pi}{2}\right) = \frac{\mathbf{D} + \mathbf{D}\cdot\boldsymbol{\lambda}\cdot\mathbf{M} + \mathbf{D}\cdot\mathbf{M} - \mathbf{M}\cdot(\boldsymbol{\lambda}+1)}{1 + \mathbf{M}\cdot\boldsymbol{\lambda} + \mathbf{M}} \\ & \Delta\mathbf{I}_{\mathbf{Lm}^{0}\mathbf{b}} = \frac{2\cdot\boldsymbol{\lambda}\cdot\mathbf{M}}{(\mathbf{M}+1)\cdot(\mathbf{D}-\mathbf{M}+\mathbf{D}\cdot\mathbf{M}-\boldsymbol{\lambda}\cdot\mathbf{M}+\mathbf{D}\cdot\boldsymbol{\lambda}\cdot\mathbf{M})} \\ & \text{sol} := \text{Minem}(\mathbf{D},\boldsymbol{\lambda}) \\ & \mathbf{D}_{v} := \text{sol}_{0} \qquad \qquad \mathbf{D} = 0.545 \\ & \mathbf{\lambda}_{v} := \text{sol}_{1} \qquad \qquad \mathbf{\lambda} = 0.153 \end{split}$$

Duty Cycle for S1 e SG:

 $q(\alpha) := M \cdot sin(\alpha)$

$$\begin{split} D_{ac}(\alpha) &\coloneqq \begin{array}{c} \frac{I_{o_barra}(\alpha) \cdot (q(\alpha) \cdot \lambda + q(\alpha) + 1) + q(\alpha) \cdot (\lambda + 1)}{q(\alpha) \cdot \lambda + q(\alpha) + 1} & \text{if } 0 < \alpha < \pi \\ \frac{-I_{o_barra}(\alpha) \cdot (-q(\alpha) \cdot \lambda - q(\alpha) + 1) - q(\alpha) \cdot (\lambda + 1)}{-q(\alpha) \cdot \lambda - q(\alpha) + 1} & \text{otherwise} \end{array} \\ \begin{array}{c} D_{ac}\left(\frac{\pi}{2}\right) &= 0.545 \\ \end{array} \end{split}$$

Duty Cycle for SP e DP:

$$\begin{split} D_{ac_SP}(\alpha) &:= \begin{array}{|c|c|} \frac{I_{o_barra}(\alpha) \cdot (q(\alpha) \cdot \lambda + q(\alpha) + 1) + q(\alpha) \cdot (\lambda + 1)}{q(\alpha) \cdot \lambda + q(\alpha) + 1} & \text{if } 0 < \alpha < \pi \\ \hline D_{ac_SP}\left(\frac{\pi}{2}\right) = 0.545 \\ \hline D_{ac_SP}\left(\frac{3\pi}{2}\right) = 0 \end{split}$$

Duty Cycle for SN e DN:

$$D_{ac_SN}(\alpha) := \begin{bmatrix} 0 & \text{if } 0 < \alpha < \pi \\ \frac{-I_{o_barra}(\alpha) \cdot (-q(\alpha) \cdot \lambda - q(\alpha) + 1) - q(\alpha) \cdot (\lambda + 1)}{-q(\alpha) \cdot \lambda - q(\alpha) + 1} & \text{otherwise} \\ \end{bmatrix} \frac{D_{ac_SN}\left(\frac{\pi}{2}\right)}{D_{ac_SN}\left(\frac{\pi}{2}\right)}$$

$$D_{ac_{SN}}\left(\frac{\pi}{2}\right) = 0$$
$$D_{ac_{SN}}\left(\frac{3\pi}{2}\right) = 0.545$$

Magnetizing Inductance Lm:

$$L_{\rm M} := \frac{L_{\rm G}}{\lambda}$$
 $L_{\rm M} =$

L_M = 26.062·µH

Voltage on Auxiliary Switching Capacitor Cg:

$$V_{CG} := \frac{D \cdot V_{IN}}{-1 + D}$$
 $V_{CG} := -83.869 V$

Minimum Current in Lm:

$$I_{1} := \frac{\lambda \cdot \left[V_{\underline{I}N} \cdot V_o \cdot (D-2) + V_o^{2} \cdot (D-1) \right] + D \cdot \left(V_{\underline{I}N} + V_o \right)^{2} - V_o \left(V_{\underline{I}N} + V_o \right)}{2\lambda \cdot f_{5} \left[V_o \cdot L_{G} + L_{M} \cdot \left(V_{\underline{I}N} + V_o \right) \right]}$$

 $\mathrm{I_l}=28.571\,\mathrm{A}$

Minimum Current in Lm (AC):

$$\begin{split} & A_{LM01}(\alpha) \coloneqq V_{IN} \cdot \frac{V_{o_AC}(\alpha)}{n} \cdot \left(\mathsf{D}_{ac}(\alpha) - 2 \right) + \left(\frac{V_{o_AC}(\alpha)}{n} \right)^2 \cdot \left(\mathsf{D}_{ac}(\alpha) - 1 \right) \\ & A_{LM02}(\alpha) \coloneqq V_{IN} \cdot \frac{-V_{o_AC}(\alpha)}{n} \cdot \left(\mathsf{D}_{ac}(\alpha) - 2 \right) + \left(\frac{-V_{o_AC}(\alpha)}{n} \right)^2 \cdot \left(\mathsf{D}_{ac}(\alpha) - 1 \right) \end{split}$$

$$\begin{split} \mathbf{I}_{1_AC}(\alpha) &\coloneqq \left| \begin{array}{l} \frac{\lambda \cdot \left(A_{\mathrm{LM01}}(\alpha) \right) + \mathbf{D}_{\mathrm{ac}}(\alpha) \cdot \left(\mathbf{V}_{\mathrm{IN}} + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right)^2 - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \cdot \left(\mathbf{V}_{\mathrm{IN}} + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right)}{n} \right| & \text{if } 0 < \alpha < \pi \\ \\ \frac{2\lambda \cdot \mathbf{f}_{5} \cdot \left[\frac{\mathbf{V}_{0_AC}(\alpha)}{n} \cdot \mathbf{L}_{G} + \mathbf{L}_{\mathrm{M}} \left(\mathbf{V}_{\mathrm{IN}} + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right) \right]}{n} & \text{if } 0 < \alpha < \pi \\ \\ \frac{\lambda \cdot \left(A_{\mathrm{LM02}}(\alpha) \right) + \mathbf{D}_{\mathrm{ac}}(\alpha) \cdot \left(\mathbf{V}_{\mathrm{IN}} - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right)^2 + \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \cdot \left(\mathbf{V}_{\mathrm{IN}} - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right)}{n} & \text{otherwise} \\ \\ \frac{2\lambda \cdot \mathbf{f}_{5} \cdot \left[\frac{-\mathbf{V}_{0_AC}(\alpha)}{n} \cdot \mathbf{L}_{G} + \mathbf{L}_{\mathrm{M}} \left(\mathbf{V}_{\mathrm{IN}} - \frac{\mathbf{V}_{0_AC}(\alpha)}{n} \right) \right]}{1 \cdot \mathbf{AC} \left(\frac{\pi}{2} \right) = 28.571 \, \mathrm{A}} \\ \end{array}$$

Máximum Current in Lm:

$$I_2 := \frac{1}{2} \cdot \frac{V_{IN} D + D \cdot V_0 - V_0}{L_G f_s}$$
 I_2 = 47.619 A

Maximum Current in Lm (AC):

$$I_{2_AC}(\alpha) := \begin{vmatrix} \frac{1}{2} \cdot \frac{V_{IN} \cdot D_{ac}(\alpha) + D_{ac}(\alpha) \cdot \frac{V_{0_AC}(\alpha)}{n} - \frac{V_{0_AC}(\alpha)}{n}}{L_G f_s} & \text{if } 0 < \alpha < \pi \\\\ \frac{1}{2} \cdot \frac{V_{IN} \cdot D_{ac}(\alpha) + D_{ac}(\alpha) \cdot \frac{-V_{0_AC}(\alpha)}{n} + \frac{V_{0_AC}(\alpha)}{n}}{L_G f_s} & \text{otherwise} \\\\ \hline\\ I_{2_AC}\left(\frac{\pi}{2}\right) = 47.619 \text{ A} \\\\ I_{2_AC}\left(\frac{3\pi}{2}\right) = 47.619 \text{ A} \end{vmatrix}$$

4. Operating Stages Duration:

1st Operating Stage (I1->I2):

$$\begin{split} \Delta t l &:= \frac{\left(I_2 - I_1\right) \cdot \left(L_G + L_M\right)}{V_{IN}} \\ \frac{1 \text{st Operating Stage (AC):}}{\Delta t l_{ac}(\alpha) := \frac{\left(I_2 _ AC(\alpha) - I_1 _ AC(\alpha)\right) \cdot \left(L_G + L_M\right)}{V_{IN}} \end{split}$$

$$\Delta t l_{ac}\left(\frac{\pi}{2}\right) = 8.18 \cdot \mu s$$

 $\Delta t l = 8.18 \cdot \mu s$

3rd Operating Stage (12->0):

$$\Delta t3 := \frac{(1 - D)}{2 \cdot f_{\star}}$$

 $\frac{3 \text{rd Operating Stage (AC):}}{\Delta t \beta_{ac}(\alpha) := \frac{\left(1 - D_{ac}(\alpha)\right)}{2 \cdot f_{c}}}$

<u>4th Operating Stage (0-> -12):</u> Δt4 := Δt3

 $\frac{\text{4th Operating Stage (AC):}}{\Delta t4_{ac}(\alpha) := \Delta t3_{ac}(\alpha)}$

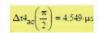
6th Operating Stage (-I2->0):

$$\Delta t6 := \frac{V_{IN} \cdot D + D \cdot V_{\circ} - V_{\circ}}{2(V_{IN} + V_{\circ}) \cdot f_{\circ}}$$

$$\Delta t3 = 4.549 \cdot \mu s$$

$$\Delta t_{ac} \left(\frac{3\pi}{2}\right) = 4.549 \cdot \mu c$$

 $\Delta t4 = 4.549 \cdot \mu s$



$\Delta t6 = 1.701 \cdot \mu s$

6th Operating Stage (AC):

$$\begin{split} \Delta t 6_{ac}(\alpha) &\coloneqq \left(\begin{array}{c} \frac{V_{\underline{I}\underline{N}^{*}}D_{ac}(\alpha) + D_{ac}(\alpha) \cdot \frac{V_{\underline{0}_\underline{A}\underline{C}}(\alpha)}{n} - \frac{V_{\underline{0}_\underline{A}\underline{C}}(\alpha)}{n}}{2\left(V_{\underline{I}\underline{N}} + \frac{V_{\underline{0}_\underline{A}\underline{C}}(\alpha)}{n}\right) \cdot \mathbf{f}_{5}} & \text{if } 0 < \alpha < \pi \\ \\ \frac{V_{\underline{I}\underline{N}^{*}}D_{ac}(\alpha) - D_{ac}(\alpha) \cdot \frac{V_{\underline{0}_\underline{A}\underline{C}}(\alpha)}{n} + \frac{V_{\underline{0}_\underline{A}\underline{C}}(\alpha)}{n}}{2\left(V_{\underline{I}\underline{N}} - \frac{V_{\underline{0}_\underline{A}\underline{C}}(\alpha)}{n}\right) \cdot \mathbf{f}_{5}} & \text{otherwise} \\ \\ \frac{\Delta t 6_{ac}\left(\frac{3\pi}{2}\right) = 1.701 \cdot \mu s}{\Delta t 6_{ac}\left(\frac{3\pi}{2}\right) = 1.701 \cdot \mu s} \end{split}$$

7th Operating Stage (0->I1):

$$\Delta t7 := \frac{L_G \cdot I_1}{V_{DN} + V_{-0}}$$

$$\Delta t7 = 1.02 \cdot \mu s$$

Sétima Etapa - Saída Alternada:

$$\begin{split} \Delta t 7_{ac}(\alpha) &\coloneqq \left| \begin{array}{c} \frac{L_{G} I_{1_AC}(\alpha)}{V_{IN} + \frac{V_{o_AC}(\alpha)}{n}} & \text{if } 0 < \alpha < \pi \\ \\ \frac{L_{G} I_{1_AC}(\alpha)}{V_{IN} - \frac{V_{o_AC}(\alpha)}{n}} & \text{otherwise} \end{array} \right| \\ \end{array} \right. \\ \left| \begin{array}{c} \Delta t 7_{ac} \left(\frac{\pi}{2} \right) = 1.02 \cdot \mu s \end{array} \right| \end{split}$$

5. Intermediate Equations:

Lm current in ∆t6

$$I_{x} := \frac{I_{1} \cdot (\Delta t3 + \Delta t4) + I_{2} \cdot (\Delta t6 + \Delta t7)}{\Delta t3 + \Delta t4 + \Delta t6 + \Delta t7}$$
$$I_{x} = 32.956 \text{ A}$$

Lm current in Δt6 (AC)

$$\begin{split} \mathrm{I}_{\mathrm{X}_\mathrm{AC}}(\alpha) &:= \frac{\mathrm{I}_{1_\mathrm{AC}}(\alpha) \cdot \left(\Delta t_{\mathrm{ac}}^{2}(\alpha) + \Delta t_{\mathrm{ac}}^{4}(\alpha)\right) + \mathrm{I}_{2_\mathrm{AC}}(\alpha) \cdot \left(\Delta t_{\mathrm{ac}}^{2}(\alpha) + \Delta t_{\mathrm{ac}}^{7}(\alpha)\right)}{\Delta t_{\mathrm{ac}}^{3}(\alpha) + \Delta t_{\mathrm{ac}}^{4}(\alpha) + \Delta t_{\mathrm{ac}}^{2}(\alpha) + \Delta t_{\mathrm{ac}}^{7}(\alpha)} \\ \mathrm{I}_{\mathrm{X}_\mathrm{AC}}\left(\frac{\pi}{2}\right) &= 32.956 \,\mathrm{A} \end{split}$$

$$\begin{split} \mathrm{I}_{\mathrm{X}_\mathrm{AC}}\left(\frac{3\pi}{2}\right) &= 32.956 \,\mathrm{A} \end{split}$$

Output Current Validation

$$\begin{split} I_{o_calc} &:= \frac{\left(I_2 + I_x\right) \cdot f_s \cdot (\Delta t3 + \Delta t4)}{2 \cdot n} + \frac{\left(I_2 + I_x\right) \cdot f_s \cdot (\Delta t6 + \Delta t7)}{2 \cdot n} \\ I_{o_calc} &= 5.568 \, \text{A} \end{split}$$

6. Auxiliary Switching Inductance Lg:

Average Current (DC) - Lg:

$$I_{LG} \coloneqq \frac{1}{T_5} \left[\int_0^{\Delta t1} \left[\frac{(I_2 - I_1) \cdot t}{\Delta t1} + I_1 \right] dt + \int_0^{\Delta t3 + \Delta t4} \left[\frac{(-2I_2) \cdot t}{(\Delta t3 + \Delta t4)} + I_2 \right] dt + \int_0^{\Delta t6 + \Delta t7} \left[\frac{(I_1 + I_2) \cdot t}{(\Delta t7 + \Delta t6)} - I_2 \right] dt \right]$$

$$I_{LG} \coloneqq 14.286 \text{ A}$$

RMS Current (DC) - Lq:

$$I_{LG_rms} := \sqrt{\frac{1}{T_{5}}} \left[\int_{0}^{\Delta t1} \left[\frac{(I_{2} - I_{1}) \cdot t}{\Delta t1} + I_{1} \right]^{2} dt + \int_{0}^{\Delta t3 + \Delta t4} \left[\frac{(-2I_{2}) \cdot t}{(\Delta t3 + \Delta t4)} + I_{2} \right]^{2} dt + \int_{0}^{\Delta t6 + \Delta t7} \left[\frac{(I_{1} + I_{2}) \cdot t}{(\Delta t7 + \Delta t6)} - I_{2} \right]^{2} dt \right] I_{LG_rms} = 32.062 \text{ A}$$

Average Current (AC) - Lq:

$$\begin{split} I_{\text{LG}_\text{AC}} &\coloneqq \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{1_\text{AC}}(\alpha) + I_{2_\text{AC}}(\alpha)\right) \cdot \Delta t I_{ac}(\alpha) + \left(I_{1_\text{AC}}(\alpha) - I_{2_\text{AC}}(\alpha)\right) \cdot \left(\Delta t 6_{ac}(\alpha) + \Delta t 7_{ac}(\alpha)\right)}{2 \cdot T_{s}} \, d\alpha \\ I_{\text{LG}_\text{AC}} &= 7.143 \, \text{A} \end{split}$$

RMS Current (AC) - Lq:

$$\begin{split} &A_{\mathrm{LG01}}(\alpha) \coloneqq \left(I_{1_AC}(\alpha)^{2} + I_{1_AC}(\alpha) \cdot I_{2_AC}(\alpha) + I_{2_AC}(\alpha)^{2}\right) \cdot \Delta t I_{ac}(\alpha) \\ &A_{\mathrm{LG02}}(\alpha) \coloneqq \left(I_{2_AC}(\alpha)^{2}\right) \cdot \left(\Delta t 3_{ac}(\alpha) + \Delta t 4_{ac}(\alpha)\right) \\ &A_{\mathrm{LG03}}(\alpha) \coloneqq \left(I_{1_AC}(\alpha)^{2} - I_{1_AC}(\alpha) \cdot I_{2_AC}(\alpha) + I_{2_AC}(\alpha)^{2}\right) \cdot \left(\Delta t 6_{ac}(\alpha) + \Delta t 7_{ac}(\alpha)\right) \\ &I_{\mathrm{LG_AC_mss}} \coloneqq \sqrt{\frac{1}{2\pi}} \cdot \int_{0}^{2\pi} \left(\frac{A_{\mathrm{LG01}}(\alpha) + A_{\mathrm{LG02}}(\alpha) + A_{\mathrm{LG03}}(\alpha)}{3 \cdot T_{s}}\right) d\alpha \\ &I_{\mathrm{LG_AC_mss}} \equiv 21.497 \, A \end{split}$$

Maximum Voltage on Lg:

$$V_{LG_{max}} := V_{IN} + \frac{V_{o_AC}\left(\frac{\pi}{2}\right)}{n}$$
$$V_{LG_{max}} = 112 V$$

7. Magnetizing Inductance Lm:

Average Lm Current (DC):

$$\begin{split} I_{LM} &\coloneqq \frac{I_1 + I_2}{2} & I_{LM} &\equiv 38.095 \text{ A} \\ \\ \text{delta_I}_{LM} &\coloneqq \frac{(I_2 - I_1) \cdot 2}{I_1 + I_2} & \text{delta_I}_{LM} &\equiv 0.5 \end{split}$$

Average Lm Current (AC):

$$I_{LM_AC} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{1_AC}(\alpha) + I_{2_AC}(\alpha)\right)}{2} d\alpha \qquad \qquad I_{LM_AC} = 22.3 \text{ A}.$$

Average Lm Current (AC):

- C

$$I_{LM_AC_RMS} \coloneqq \sqrt{\frac{1}{2\pi}} \cdot \int_{0}^{2\pi} \left[\frac{(I_{1_AC}(\alpha) + I_{2_AC}(\alpha))}{2} \right]^{2} d\alpha \quad I_{LM_AC_RMS} \equiv 25.469 \text{ A}$$

Maximum voltage on Lm:

$$V_{LM_{max}} \coloneqq V_{IN} - \frac{L_G V_{IN}}{L_G + L_M} \qquad \qquad V_{LM_{max}} \equiv 60.686 V$$

8. Auxiliary Switching Capacitor - Cg:

Desired Voltage Ripple:

$$\Delta V_{CG} := V_{CG} \cdot \Delta V_{CG\%} \qquad \qquad \Delta V_{CG} = -54.515 \cdot V$$

Capacitance:

$$C_{G} := \frac{-I_{2} \cdot \Delta t_{3}}{2 \cdot \Delta V_{CG}}$$

$$C_{G} = 1.987 \cdot \mu F$$

Average Current (DC) - Cq:

$$\begin{split} I_{CG} &\coloneqq \frac{1}{T_s} \cdot \int_0^{\Delta t 3 + \Delta t 4} \left[\frac{(I_2 + I_2) \cdot t}{\Delta t 3 + \Delta t 4} - I_2 \right] dt \\ I_{CG} &= 0. A \end{split}$$

RMS Current (DC) - Cq:

$$\begin{split} I_{\text{CG}_\text{Ims}} & \coloneqq \sqrt{\frac{1}{T_s}} \cdot \int_0^{\Delta t 3 + \Delta t 4} \left[\frac{(I_2 + I_2) \cdot t}{\Delta t 3 + \Delta t 4} - I_2 \right]^2 dt \\ I_{\text{CG}_\text{Ims}} & = 18.544 \, \text{A} \end{split}$$

Average Current (AC) - Cq:

$$I_{CG_AC} = \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \left[\frac{-I_{2_AC}(\alpha) \cdot \left(\Delta t^{3}_{ac}(\alpha) - \Delta t^{4}_{ac}(\alpha) \right)}{2T_{5}} \right] d\alpha$$

$$I_{CG_AC} = 0 A$$

RMS Current (AC) - Cq:

$$I_{CG_AC_RMS} := \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} \left[\frac{I_{2_AC}(\alpha)^2 \cdot \left(\Delta t^3_{ac}(\alpha) + \Delta t^4_{ac}(\alpha)\right)}{3T_s} \right] d\alpha$$
$$I_{CG_AC_RMS} = 13.508 \text{ A}$$

9. Main Switch - S1:

Average Current (DC) - S1:

 $I_{S1} := I_{CG} + I_{LG}$

$$I_{S1} = 14.286 \text{ A}$$

RMS Current (DC) - S1:

$$I_{S1_rms} := \sqrt{\frac{1}{T_s}} \left[\int_0^{\Delta t1} \left[\frac{(I_2 - I_1) \cdot t}{\Delta t1} + I_1 \right]^2 dt + \int_0^{\Delta t6 + \Delta t7} \left[\frac{(I_2 + I_1) \cdot t}{\Delta t6 + \Delta t7} - I_2 \right]^2 dt \right]$$

$$I_{S1_rms} = 26.155 \text{ A}.$$

Average Current (AC) - S1:

$$I_{S1_AC} := \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\left(I_{1_AC}(\alpha) + I_{2_AC}(\alpha)\right) \cdot \Delta t I_{ac}(\alpha) + \left(I_{1_AC}(\alpha) - I_{2_AC}(\alpha)\right) \cdot \left(\Delta t f_{ac}(\alpha) + \Delta t T_{ac}(\alpha)\right)}{2 \cdot T_{s}} d\alpha$$

$$I_{S1_AC} = 7.143 \text{ A}$$

RMS Current (AC) - S1:

$$I_{S1_AC_RMS} \coloneqq \sqrt{\frac{1}{2\pi}} \cdot \int_{0}^{2\pi} \frac{\left(I_{1_AC}(\alpha) + I_{2_AC}(\alpha)\right)^{2} \cdot \Delta t I_{ac}(\alpha) + \left(I_{1_AC}(\alpha) - I_{2_AC}(\alpha)\right)^{2} \cdot \left(\Delta t \delta_{ac}(\alpha) + \Delta t 7_{ac}(\alpha)\right)}{3 \cdot T_{s}} d\alpha$$

$$I_{S1_AC_RMS} \equiv 18.176 \text{ A}$$

$$\frac{Maximum Voltage - S1:}{V_{S1_max}} \approx V_{IN} - V_{CG} - \frac{\Delta V_{CG}}{2}$$

$$\frac{V_{S1_max} = 181.127 \text{ V}}{V_{S1_max}} = 181.127 \text{ V}$$

10. Auxiliary Switch - Sg:

Average Current (DC) - Sq:

 $I_{SG} := I_{CG}$ $I_{SG} = 0 A$

RMS Current (DC) - Sq:

 $I_{SG_{max}} := I_{CG_{max}}$

I_{SG_Ims} = 18.544 A

Average Current (AC) - Sq:

 $I_{SG_AC} := I_{CG_AC}$

 $I_{SG_AC} = 0A$

RMS Current (AC) - Sq:

ISG_AC_RMS := ICG_AC_RMS

I_{SG_AC_RMS} = 13.508 A

Maximum Voltage - SG:

 $V_{SG_{max}} := V_{S1_{max}}$

V_{SG max} = 181.127 V

11. Output Filter Capacitor Co:

Desired Voltage Ripple:

 $\Delta V_o := V_o \cdot \Delta V_{o\%}$

 $\Delta V_o = 30.533 \cdot V$

Capacitance:

$$C_o := \frac{I_o_{max} \cdot D}{\Delta V_o \cdot f_s}$$

 $C_o = 1.988 \cdot \mu F$

12. Blocking Diode DP:

Average Current (DC) - Dp:

 $I_{DP} := I_{o_cale}$ $I_{DP} = 5.568 A$ RMS Current (DC) - Dp:

$$I_{DP_mmc} := \sqrt{\frac{1}{T_5}} \left[\int_0^{\Delta t3 + \Delta t4} \left[\frac{\left(\frac{I_2}{n} + \frac{I_x}{n}\right) \cdot t}{\Delta t3 + \Delta t4} \right]^2 dt + \int_0^{\Delta t6 + \Delta t7} \left[\frac{\left(\frac{-I_2}{n} - \frac{I_x}{n}\right) \cdot t}{\Delta t6 + \Delta t7} + \frac{I_2}{n} + \frac{I_x}{n} \right]^2 dt \right]$$

$$I_{DP_mmc} = \$.363 A$$

Average Current (AC) - Dp:

$$\begin{split} I_{DP_AC} &:= \frac{1}{2\pi} \cdot \int_{0}^{\pi} \frac{\left(I_{x_AC}(\alpha) + I_{2_AC}(\alpha)\right) \cdot \left(\Delta t \beta_{ac}(\alpha) + \Delta t 4_{ac}(\alpha) + \Delta t 6_{ac}(\alpha) + \Delta t 7_{ac}(\alpha)\right)}{2T_{s} \cdot n} \, d\alpha \\ I_{DP_AC} &= 1.772 \, A \end{split}$$

RMS Current (AC) - Dp:

$$I_{DP_AC_RMS} \coloneqq \sqrt{\frac{1}{2\pi}} \int_{0}^{\pi} \frac{\left(I_{x_AC}(\alpha) + I_{2_AC}(\alpha)\right)^{2} \cdot \left(\Delta t_{ac}(\alpha) + \Delta t_{ac}(\alpha) + \Delta t_{ac}(\alpha) + \Delta t_{ac}(\alpha) + \Delta t_{ac}(\alpha)\right)}{3T_{s} \cdot n^{2}} d\alpha$$

IDP_AC_RMS = 4.05 A

Maximum Voltage - Dp:

$$V_{DP_{max}} := V_{o_AC}\left(\frac{\pi}{2}\right) + V_{o_AC}\left(\frac{\pi}{2}\right) \Delta V_{o\%} + V_{LM_{max}} n$$
$$V_{DP_{max}} = 469.651 V$$

13. Blocking Diode DN:

Average Current (DC) - Dn:

I_{DN} := 0A

 $I_{DN} = 0$

RMS Current (DC) - Dn:

I_{DN ms} := 0A

 $I_{DN_{ms}} = 0$

Average Current (AC) - Dn:

$$\begin{split} I_{\text{DN_AC}} &= \frac{1}{2\pi} \cdot \int_{\pi}^{2\pi} \frac{\left(I_{x_AC}(\alpha) + I_{2_AC}(\alpha)\right) \cdot \left(\Delta t \beta_{ac}(\alpha) + \Delta t 4_{ac}(\alpha) + \Delta t 6_{ac}(\alpha) + \Delta t 7_{ac}(\alpha)\right)}{2T_{5} \cdot n} \, d\alpha \\ I_{\text{DN_AC}} &= 1.772 \text{ A} \end{split}$$

$$I_{DN_AC_RMS} := \sqrt{\frac{1}{2\pi}} \int_{\pi}^{2\pi} \frac{\left(I_{x_AC}(\alpha) + I_{2_AC}(\alpha)\right)^2 \cdot \left(\Delta t_{ac}^3(\alpha) + \Delta t_{ac}^4(\alpha) + \Delta t_{ac}^6(\alpha) + \Delta t_{ac}^7(\alpha)\right)}{3T_{s'}n^2} d\alpha$$

$$I_{DN_AC_RMS} = 4.05 \text{ A}$$

Maximum Voltage - Dn:

$$V_{\text{DN}_{\text{max}}} := -V_{o_AC} \left(\frac{3\pi}{2}\right) - V_{o_AC} \left(\frac{3\pi}{2}\right) \cdot \Delta V_{o\%} + V_{\text{LM}_{\text{max}} \cdot n}$$
$$V_{\text{DN}_{\text{max}}} = 469.651 \text{ V}$$

14. Switch SP:

Average Current (DC) Sp:

 $I_{SP} := I_{o_{calc}}$

I_{SP} = 5.568 A

RMS Current (DC) - Sp:

 $I_{SP_ms} := I_{DP_ms}$

I_{SP_rms} = 8.363 A

Average Current (AC) - Sp:

 $I_{SP_AC} := I_{DP_AC}$

I_{SP AC} = 1.772 A

RMS Current (AC) - Sp:

 $I_{SP_AC_RMS} := I_{DP_AC_RMS}$

 $I_{SP_AC_RMS} = 4.05 A$

APPENDIX I

APPENDIX I - CALCULATION OF LOSSES FOR THE DC-AC ACTIVE- CLAMPING FLYBACK CONVERTER – COMPLEMENTARY SWITCHING 100 KHZ

DC-AC Active-clamping Flyback Converter - Calculation of

Losses 100 kHz	ter - Calculation of
Specifications:	
P _o := 500W	
V _{IN} := 70V	
V _{o_RMS} := 127V	
$f_5 := 100 kHz$	
$L_G := 2\mu H$	
L _M := 22.219 μH	
n := 4.276	
Peak Output Voltage:	
$V_{o_max} := \sqrt{2} \cdot V_{o_RMS}$	V _{o_max} = 179.605 V
Output Current (Linear Load):	
$I_{o_max} := \frac{2 \cdot P_o}{V_o_max}$	I _{0_max} = 5.568 A
o_max V _{o_max}	-o_max
$I_0(\alpha) := I_{0_max} \cdot \sin(\alpha)$	
Parameterized Output Current:	
$\mathbf{I_{o_param}}(\alpha) \coloneqq \frac{2 \cdot \mathbf{f_{s}} \cdot \mathbf{L_{G}} \cdot \mathbf{n}}{V_{IN}} \cdot \mathbf{I_{o}}(\alpha)$	
Modulation Index:	
$M := \frac{V_{o_max}}{n \cdot V_{IN}}$	M = 0.6
Equivalent Output Resistance:	
$R_o := \frac{V_o_max}{I_o_max}$	$R_0 = 32.258 \Omega$
¹ o_max	
Voltage Conversion Ratio:	
$q(\alpha) := M \cdot sin(\alpha)$	
Inductance Factor:	
$\lambda := \frac{L_G}{L_M}$	λ = 0.09

Duty Cycle:

$$\begin{split} D(\alpha) &\coloneqq & I_{o_param}(\alpha) + \frac{q(\alpha) + \lambda \cdot q(\alpha)}{q(\alpha) + \lambda \cdot q(\alpha) + 1} & \text{if } \alpha \leq \pi \\ & I_{o_param}(\alpha - \pi) + \frac{q(\alpha - \pi) + \lambda \cdot q(\alpha - \pi)}{q(\alpha - \pi) + \lambda \cdot q(\alpha - \pi) + 1} & \text{if } \alpha > \pi \end{split}$$

Active-clamping Capacitor Voltage:

$$V_{CG}(\alpha) := \frac{D(\alpha) \cdot V_{IN}}{(1 - D(\alpha))}$$
$$V_{CG_max} := V_{CG}\left(\frac{\pi}{2}\right)$$
$$V_{CG_max} = 79.403 V$$

Current Values:

$$I_2(\alpha) := \frac{[D(\alpha) \cdot (1 + q(\alpha)) - q(\alpha)] \cdot V_{\underline{IN}}}{2 \cdot f_5 \cdot L_{\underline{G}}}$$

$$I_{1}(\alpha) := \frac{\left[(\lambda \cdot D(\alpha) + D(\alpha) - \lambda - 1) \cdot q(\alpha)^{2} + (\lambda \cdot D(\alpha) + 2D(\alpha) - 2 \cdot \lambda - 1) \cdot q(\alpha) + D(\alpha) \right] \cdot V_{\underline{IN}}}{2 \cdot f_{5} \cdot L_{\underline{G}^{*}}(\lambda \cdot q(\alpha) + 1 + q(\alpha))} \qquad \qquad I_{1}\left(\frac{\pi}{2}\right) = \frac{\left[(\lambda \cdot D(\alpha) + D(\alpha) - \lambda - 1) \cdot q(\alpha) + D(\alpha) - 2 \cdot \lambda - 1 \right] \cdot q(\alpha)}{2 \cdot f_{5} \cdot L_{\underline{G}^{*}}(\lambda \cdot q(\alpha) + 1 + q(\alpha))}$$

$$I_{x}(\alpha) \coloneqq \frac{\left[(2 \cdot \lambda \cdot D(\alpha) + D(\alpha) - 2 \cdot \lambda - 1) \cdot q(\alpha) + D(\alpha)\right] \cdot V_{\overline{IN}}}{2 \cdot f_{5} \cdot L_{G}}$$

Duration of the Operating Stages:

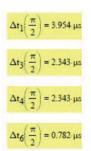
$$\begin{split} \Delta t_1(\alpha) &\coloneqq \frac{q(\alpha) \cdot (1 + \lambda)}{f_5 \cdot (\lambda \cdot q(\alpha) + 1 + q(\alpha))} \\ \Delta t_3(\alpha) &\coloneqq \frac{(1 - D(\alpha))}{2 \cdot f_5} \\ \Delta t_4(\alpha) &\coloneqq \frac{(1 - D(\alpha))}{2 \cdot f_5} \end{split}$$

$$\Delta t_6(\alpha) := \frac{D(\alpha) \cdot (1 + q(\alpha)) - q(\alpha)}{2 \cdot f_5 \cdot (1 + q(\alpha))}$$

$$\Delta t_7(\alpha) := \frac{(\lambda \cdot D(\alpha) + D(\alpha) - \lambda - 1) \cdot q(\alpha)^2 + (\lambda \cdot D(\alpha) + 2D(\alpha) - 2 \cdot \lambda - 1) \cdot q(\alpha) + D(\alpha)}{2 \cdot f_5 \cdot (1 + q(\alpha)) \cdot (\lambda \cdot q(\alpha) + 1 + q(\alpha))}$$

Current in the Magnetizing Inductance:

 $\Delta I_{\underline{LM}}(\alpha) \coloneqq \left[\frac{V_{\underline{IN}} \cdot \lambda \cdot q(\alpha)}{L_{G} \cdot f_{5} \cdot (q(\alpha) + \lambda \cdot q(\alpha) + 1)} \right]$



 $I_2\left(\frac{\pi}{2}\right) = 43.808 \,\text{A}$

 $I_x\left(\frac{\pi}{2}\right) = 34.951 \text{ A}$

= 32.379 A



$$\Delta I_{LM_max} \coloneqq \Delta I_{LM}\left(\frac{\pi}{2}\right) \qquad \Delta I_{LM_max} = 11.429 \text{ A}$$
$$I_{LM}(\alpha) \coloneqq \left[\frac{V_{IN}(q(\alpha) + 1) \cdot (D(\alpha) - q(\alpha) + D(\alpha) \cdot q(\alpha) - \lambda \cdot q(\alpha) + D(\alpha) \cdot \lambda \cdot q(\alpha))}{2 \cdot L_{G} \cdot f_{5} \cdot (q(\alpha) + \lambda \cdot q(\alpha) + 1)}\right]$$

 $I_{LM_max} := I_{LM} \left(\frac{\pi}{2}\right) + \frac{\Delta I_{LM_max}}{2} \qquad \qquad I_{LM_max} = 43.808 \text{ A}$

Average Current in the Semiconductors:

$$\begin{split} \mathbf{I}_{\begin{array}{c} S1_avg} &\coloneqq \frac{1}{\pi} \cdot \int_{0}^{\pi} \frac{\mathbf{f}_{5}}{2} \cdot \left[\left[\mathbf{I}_{1}(\boldsymbol{\omega}) - \mathbf{I}_{2}(\boldsymbol{\omega}) \right) \cdot \left(\Delta t_{6}(\boldsymbol{\omega}) + \Delta t_{7}(\boldsymbol{\omega}) \right) + \left(\mathbf{I}_{1}(\boldsymbol{\omega}) + \mathbf{I}_{2}(\boldsymbol{\omega}) \right) \cdot \Delta t_{1}(\boldsymbol{\omega}) \right] d\boldsymbol{\omega} \\ \mathbf{I}_{\begin{array}{c} S1_avg} &= 7.143 \text{ A} \end{split} \end{split}$$

$$\begin{split} I_{SG_avg} &\coloneqq \frac{1}{\pi} \cdot \int_{0}^{\pi} \frac{f_{s}}{2} \left[\left(I_{2}(\alpha) - I_{2}(\alpha) \right) \cdot \left(\Delta t_{3}(\alpha) + \Delta t_{4}(\alpha) \right) \right] d\alpha \\ I_{SG_avg} &= 0 \, A \end{split}$$

$$\begin{split} I_{SP_avg} &:= \frac{1}{2\pi} \cdot \int_{0}^{\pi} \frac{f_{s}}{2} \cdot \left[\left(\frac{I_{x}(\alpha) + I_{2}(\alpha)}{n} \right) \cdot \left(\frac{1}{f_{s}} - \Delta t_{1}(\alpha) \right) \right] d\alpha \\ I_{SP_avg} &= 1.772 \text{ A} \\ I_{SN_avg} &:= \frac{1}{2\pi} \cdot \int_{0}^{\pi} \frac{f_{s}}{2} \cdot \left[\left(\frac{I_{x}(\alpha) + I_{2}(\alpha)}{n} \right) \cdot \left(\frac{1}{f_{s}} - \Delta t_{1}(\alpha) \right) \right] d\alpha \\ I_{SN_avg} &= 1.772 \text{ A} \end{split}$$

IDP_avg := ISP_avg

I_{DP_avg} = 1.772 A

IDN_avg := ISN_avg

I_{DN_avg} = 1.772 A

$$I_{S1_RMS} \coloneqq \sqrt{\frac{1}{\pi}} \left[\int_{0}^{\pi} \frac{f_{s}}{3} \left[\left(I_{1}(\alpha)^{2} - I_{1}(\alpha) \cdot I_{2}(\alpha) + I_{2}(\alpha)^{2} \right) \cdot \left(\Delta t_{6}(\alpha) + \Delta t_{7}(\alpha) \right) + \left(I_{1}(\alpha)^{2} + I_{1}(\alpha) \cdot I_{2}(\alpha) + I_{2}(\alpha)^{2} \right) \cdot \Delta t_{1}(\alpha) \right] d\alpha \right]$$

$$I_{S1_RMS} \equiv 16.228 A$$

$$I_{SG_RMS} \coloneqq \sqrt{\frac{1}{\pi}} \left[\int_{0}^{\pi} \frac{f_{s}}{3} \left[\left(I_{2}(\alpha)^{2} - I_{2}(\alpha) \cdot I_{2}(\alpha) + I_{2}(\alpha)^{2} \right) \cdot \left(\Delta t_{3}(\alpha) + \Delta t_{4}(\alpha) \right) \right] d\alpha \right]$$

$$I_{SG_RMS} \equiv \sqrt{\frac{1}{\pi}} \left[\int_{0}^{\pi} \frac{f_{s}}{3} \left[\left(\frac{I_{x}(\alpha) + I_{2}(\alpha)}{n} \right)^{2} \cdot \left(\frac{1}{f_{s}} - \Delta t_{1}(\alpha) \right) \right] d\alpha \right]$$

$$I_{SP_RMS} \coloneqq \sqrt{\frac{1}{2\pi}} \left[\int_{0}^{\pi} \frac{f_{s}}{3} \left[\left(\frac{I_{x}(\alpha) + I_{2}(\alpha)}{n} \right)^{2} \cdot \left(\frac{1}{f_{s}} - \Delta t_{1}(\alpha) \right) \right] d\alpha \right]$$

$$I_{SN_RMS} \approx \sqrt{\frac{1}{2\pi}} \left[\int_{0}^{\pi} \frac{f_{s}}{3} \left[\left(\frac{I_{x}(\alpha) + I_{2}(\alpha)}{n} \right)^{2} \cdot \left(\frac{1}{f_{s}} - \Delta t_{1}(\alpha) \right) \right] d\alpha \right]$$

 $I_{SN_RMS} = 4.009 \text{ A}$

IDP_RMS := ISP_RMS

 $I_{DP_RMS} = 4.009 A$

IDN_RMS := ISN_RMS

I_{DN_RMS} = 4.009 A

Current in Lg:

$$\begin{split} & A_{LG01}(\alpha) \coloneqq \left(I_1(\alpha)^2 + I_1(\alpha) \cdot I_2(\alpha) + I_2(\alpha)^2\right) \cdot \Delta t_1(\alpha) \\ & A_{LG02}(\alpha) \coloneqq \left(I_2(\alpha)^2 - I_2(\alpha) \cdot I_2(\alpha) + I_2(\alpha)^2\right) (\Delta t_3(\alpha) + \Delta t_4(\alpha)) \\ & A_{LG03}(\alpha) \coloneqq \left(I_1(\alpha)^2 - I_1(\alpha) \cdot I_2(\alpha) + I_2(\alpha)^2\right) \cdot (\Delta t_6(\alpha) + \Delta t_7(\alpha)) \end{split}$$

$I_{LG_RMS} \coloneqq \sqrt{\frac{1}{\pi}} \left[\int_{0}^{\pi} \frac{\mathbf{f}_{5}}{3} \cdot \left(A_{LG03}(\alpha) + A_{LG01}(\alpha) + A_{LG02}(\alpha) \right) d\alpha \right]$	
$I_{LG_{RMS}} = 20.451 \text{A}$	
$I_{LG_{max}} := I_2\left(\frac{\pi}{2}\right)$	I _{LG_max} = 43.808 A
$\Delta I_{LG_max} \coloneqq I_2 \left(\frac{\pi}{2}\right) + I_2 \left(\frac{\pi}{2}\right)$	$\Delta I_{LG_{max}} = 87.616 \text{ A}$

RMS Current in both windings of the coupled inductor:

I _{T_prim_RMS} := I _{LG_RMS}	$I_{T_prim_RMS} = 20.451 \text{ A}$
$I_{T_sec_RMS} \coloneqq I_{DP_RMS}$	I _{T_sec_RMS} = 4.009 A

Maximum Voltage over the semiconductors:

$V_{S1}(\alpha) \coloneqq V_{\overline{IN}} + V_{CG}(\alpha)$	
$V_{S1_max} = V_{S1}\left(\frac{\pi}{2}\right)$	V _{S1_max} = 149.403 V
$V_{SG}(\alpha) \coloneqq V_{IN} + V_{CG}(\alpha)$	
$V_{SG_max} := V_{S1}\left(\frac{\pi}{2}\right)$	V _{SG_max} = 149.403 V
$V_{SP}(\alpha) := 2 \cdot n \cdot q(\alpha) \cdot V_{IN}$	
$V_{SP_max} := V_{SP}\left(\frac{\pi}{2}\right)$	V _{SP_max} = 359.21 V
$V_{\underline{SN}}(\alpha) := 2 \cdot n \cdot q(\alpha) \cdot V_{\underline{IN}}$	
$V_{SN_max} := V_{SN}\left(\frac{\pi}{2}\right)$	V _{SN_max} = 359.21 V
$V_{DP}(\alpha) := n \cdot \left(q(\alpha) + \frac{1}{1 + \lambda}\right) \cdot V_{IN}$	
$V_{DP_max} := V_{DP}\left(\frac{\pi}{2}\right)$	V _{DP_max} = 454.207 V
$V_{DN}(\boldsymbol{\omega}) \coloneqq \mathbf{n} \cdot \left(\mathbf{q}(\boldsymbol{\omega}) + \frac{1}{1 + \lambda} \right) \cdot V_{DN}$	
$V_{DN_max} := V_{DN}\left(\frac{\pi}{2}\right)$	V _{DN_max} = 454.207 V

Semiconductors:

Switches S1 e SG: IRFP4668PBF (MOSFET) Switches SP e SN: IKW40N65F5 (IGBT) Diodes DP e DN: C3D06060A Calculation of Losses: $R_{DSon} := 0.009\Omega + 0.012\Omega \cdot \frac{P_o}{500W}$ $V_{THOIGBT} := 1.25V$ $R_{onIGBT} := 0.01\Omega$ V_{TOD} := 0.85V $R_{D} := 0.125\Omega$ P_{S1 cond} := R_{DSon}·I_{S1 RMS}² $P_{S1_{cond}} = 5.53 W$ P_{SG_cond} = 3.253 W PSG_cond = RDSon ISG RMS $P_{SP_cond} = 2.376 W$ PSP_cond := VTH0IGBT ISP_avg + RonIGBT ISP_RMS PSN_cond := VTH0IGBT ISN_avg + RonIGBT ISN RMS² P_{SN cond} = 2.376 W PSW cond = PS1_cond + PSG_cond + PSP_cond + PSN_cond P_{SW_cond} = 13.535 W $P_{S1 sw} = 0$ $P_{S1 sw} := 0$ $P_{SG_sw} := 0$ $P_{SG sw} = 0$ $P_{SP sw} = 0$ $P_{SP \ sw} := 0$ $P_{SN sw} := 0$ $P_{SN sw} = 0$ $P_{SW_{sw}} = P_{S1_{sw}} + P_{SG_{sw}} + P_{SP_{sw}} + P_{SN_{sw}}$ $P_{SW_{sw}} = 0$ PSW_total := PSW_cond + PSW_sw P_{SW_total} = 13.535 W $P_{DP \text{ cond}} = V_{T0D} I_{DP \text{ avg}} + R_D I_{DP \text{ RMS}}^2$ PDP cond = 3.515 W PDN_cond = VTOD IDN_avg + RD IDN_RMS² P_{DN cond} = 3.515W $P_{D_{cond}} = 7.03 W$ $P_{D_cond} := P_{DP_cond} + P_{DN_cond}$

$P_{DP_{5W}} \coloneqq 0$	$P_{DP_sw} = 0$
$P_{DN_{sw}} := 0$	$P_{DN_{sw}} = 0$
$P_{D_{sw}} \coloneqq P_{DP_{sw}} + P_{DN_{sw}}$	$P_{D_{sw}} = 0$
$P_{D_total} := P_{D_cond} + P_{D_sw}$	$P_{D_{total}} = 7.03 W$
$R_{LG_{cu}} := 2.698 \cdot 10^{-3} \Omega$	
$P_{LG_cond} := R_{LG_cu} I_{LG_RMS}^2$	$P_{LG_cond} = 1.128 W$
$P_{LG_mag} = 1.021W \cdot \frac{P_o}{500W}$	$P_{LG_mag} = 1.021 W$
$P_{LG} := P_{LG_cond} + P_{LG_mag}$	$P_{LG} = 2.149 W$
$R_{LM_cu_pri} := 6.3 \cdot 10^{-3} \cdot \Omega$	
$R_{LM_cu_sec} := 123 \cdot 10^{-3} \cdot \Omega$	
$P_{LM_pri_cond} := R_{LM_cu_pri} I_{T_prim_RMS}^2$	P _{LM_pri_cond} = 2.635W
$P_{LM_sec_cond} \coloneqq R_{LM_cu_sec} I_{T_sec_RMS}^2$	$P_{LM_sec_cond} = 1.977 W$
PLM_mag := 0.287W	
$P_{LM} := P_{LM_pri_cond} + 2P_{LM_sec_cond} + P_{LM_mag}$	$P_{LM} = 6.875 W$
$R_{clamp_sec} \coloneqq 100 k\Omega$	
$V_{elamp_sec} := 520V + 60V \cdot \frac{P_o}{500W}$	
$P_{clamp_sec} \coloneqq \frac{2 \cdot V_{clamp_sec}^2}{R_{clamp_sec}}$	P _{clamp_sec} = 6.728W
Efficiency Estimation:	
$\eta := \frac{P_0}{P_0}$	$\eta = 93.228.\%$
$P + P_{} + P_{} + P_{} + P_{} + P_{}$	

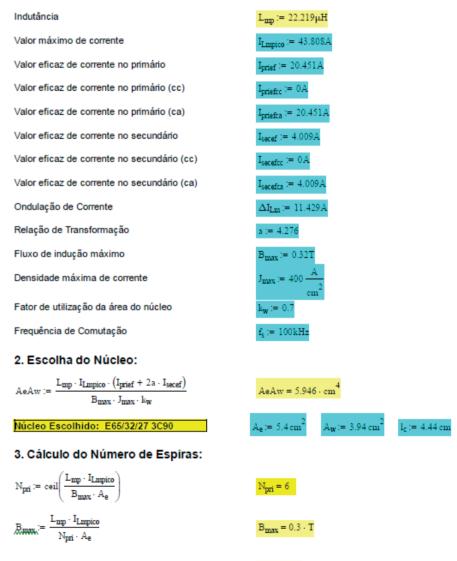
 $\eta := \frac{1}{P_o + P_{SW_total} + P_{D_total} + P_{LG} + P_{LM} + P_{clamp_sec}}$

APPENDIX J

APPENDIX J - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER - COUPLED INDUCTOR 100 KHZ

Projeto Físico do Indutor Lm - Conversor CC-CA Flyback com GA

1.Especificações:



$N_{sec} =$	26
-------------	----

4. Cálculo do entreferro:

$$l_{entreferro} := \frac{N_{pri}^{2} \cdot \mu_{0} \cdot A_{e} \cdot \left(10^{-2} \cdot \frac{m}{cm}\right)}{L_{mp}}$$

$$l_{entreferro} = 1.099 \cdot mm$$

5. Cálculo da bitola do condutor:

- T_{max} := 100
- $\eta_W := 0.8$

$$\rho_{T} \coloneqq 17.9 \cdot 10^{-9} \cdot \left[1 + 0.0039 (T_{max} - 20)\right] \cdot \Omega \cdot \mathbf{m}$$

 $\boldsymbol{\delta}_{W} := \sqrt{\frac{\boldsymbol{\rho}_{T}}{\boldsymbol{\pi} \cdot \boldsymbol{\mu}_{0} \cdot \mathbf{f}_{s}}}$

Diâmetro do Fio:

 $D_{fio} := 2 \cdot \delta_W$

dw:= 0.10mm

 $S_{fio} := 0.000080 \cdot cm^2$

$$\begin{split} n_{\text{condpri}} &\coloneqq \operatorname{ceil}\!\left(\frac{S_{\text{cohrepri}}}{S_{\text{fio}}}\right) \\ x &\coloneqq \operatorname{ceil}\!\left(\frac{n_{\text{condpri}}}{41}\right) \end{split}$$

Aconducia = 41 · x

$$\begin{split} S_{\text{cobresec}} &:= \frac{I_{\text{secef}}}{J_{\text{max}}} \\ n_{\text{condsec}} &:= \text{ceil} \bigg(\frac{S_{\text{cobresec}}}{S_{\text{fin}}} \bigg) \end{split}$$

 $S_{fioiso} := 0.000130 \cdot cm^2$ $S_{cobrepri} = 0.051 \cdot cm^2$ $n_{condpri} = 640$

 $\delta_{nr} = 0.244 \cdot mm$

 $D_{fio} = 0.049 \cdot cm$

dw_iso := 0.13mm

x = 16

n_{condpri} = 656

 $S_{cobresec} = 0.01 \cdot cm^2$

 $n_{condsec} = 126$

$$x_{i} = \operatorname{ceil}\left(\frac{n_{condsec}}{41}\right)$$

x = 4

 $\mathcal{H}_{\text{condsec}} := 41 \cdot x$

 $n_{condsec} = 164$

l_{fiopri} = 0.9 m

l_{fiosec} = 3.9 m

 $R_{ccsec} = 0.07 \cdot \Omega$

 $\Delta = 0.306$

 $R_{ccori} = 4.027 \times 10^{-3} \cdot \Omega$

6. Cálculo das Perdas:

6.1 Perdas no Cobre:

l_{espira} := 15cm

 $l_{fiopri} := N_{pri} \cdot l_{espira}$

 $R_{ccpri} \coloneqq \frac{\rho_{fio} \cdot l_{espira} \cdot N_{pri}}{n_{condpri}}$

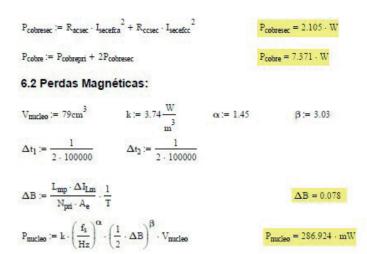
 $l_{flosec} := N_{sec} \cdot l_{espira}$

$$\begin{split} & \mathbf{R}_{\mathsf{ccsec}} \coloneqq \frac{\rho_{\mathsf{fio}} \cdot \mathbf{l}_{\mathsf{espira}} \cdot \mathbf{N}_{\mathsf{sec}}}{n_{\mathsf{condsec}}} \\ & \Delta \coloneqq \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \cdot \frac{\mathbf{d}_{\mathsf{W}}}{\delta_{\mathsf{W}}} \cdot \sqrt{\eta_{\mathsf{W}}} \end{split}$$

$$F_{\mathbf{r}} \coloneqq \Delta \cdot \left[\frac{e^{2\Delta} - e^{-2\cdot\Delta} + 2\cdot\sin(2\cdot\Delta)}{e^{2\cdot\Delta} + e^{-2\cdot\Delta} - 2\cdot\cos(2\cdot\Delta)} + \frac{2}{3} \cdot \left(N_{cam}^2 - 1 \right) \cdot \frac{e^{\Delta} - e^{-\Delta} - 2\cdot\sin(\Delta)}{e^{\Delta} + e^{-\Delta} + 2\cdot\cos(\Delta)} \right]$$

$$F_{I} = 1.876$$

$$\begin{split} & R_{acpri} \coloneqq F_r \cdot R_{ccpri} & R_{acpri} = 7.557 \times 10^{-3} \cdot \Omega \\ & R_{acsec} \coloneqq F_r \cdot R_{ccsec} & R_{acsec} = 0.131 \cdot \Omega \\ & P_{cobrepri} \coloneqq R_{acpri} \cdot I_{priefca}^{2} + R_{ccpri} \cdot I_{priefcc}^{2} & P_{cobrepri} = 3.161 \cdot W \end{split}$$



$$\begin{split} \mathbf{k}_{\mathbf{i}} &\coloneqq \frac{\mathbf{k}}{\left(2 \cdot \pi\right)^{\alpha - 1} \cdot 2^{\beta - \alpha}} \cdot \int_{0}^{2\pi} \left(\left|\cos(\theta)\right|\right)^{\alpha} d\theta} \\ \mathbf{P}_{\mathbf{v}} &\coloneqq \left(\frac{\mathbf{f}_{\mathbf{s}}}{Hz}\right) \cdot \mathbf{k}_{\mathbf{i}} \cdot \left(\Delta B\right)^{\beta - \alpha} \cdot 2 \left[\int_{0}^{\Delta t_{1}} \left(\frac{\Delta B}{2\Delta t_{1}}\right)^{\alpha} dt + \int_{0}^{\Delta t_{2}} \left(\frac{\Delta B}{2\Delta t_{2}}\right)^{\alpha} dt\right] \\ \mathbf{P}_{\mathbf{v}} &= 2.453 \cdot \frac{\mathbf{k}W}{\mathbf{m}^{3}} \\ \mathbf{Runcleo}_{\mathbf{i}} &\coloneqq \mathbf{P}_{\mathbf{v}} \cdot \mathbf{V}_{\mathbf{m}cleo} \\ \end{split}$$

6.3 Perdas Totais:

Ptotais := Pcobre + Pnucleo

 $P_{totais} = 7.565 \cdot W$

6.4 Resistência Térmica do Núcleo:

$$Rt_{mcleo} \coloneqq 23 \cdot \frac{K}{W} \left(\frac{A_e A_w}{cm^4} \right)^{-0.37} Rt_{mcleo} = 7.42 \cdot \frac{K}{W}$$

6.5 Elevação de Temperatura:

$$\Delta T := (P_{cobre} + P_{nucleo})Rt_{nucleo}$$

 $\Delta T = 56.132 \, \text{K}$

7. Possibilidade de Execução:

$$\begin{array}{ll} A_{w_min} \coloneqq \frac{N_{pri} \cdot S_{fioiso} \cdot n_{condpri} + 2N_{sec} \cdot S_{fioiso} \cdot n_{condsec}}{k_w} & A_{w_min} = 2.315 \cdot cm^2 \end{array}$$

$$Exec \coloneqq \frac{A_{w_min}}{A_w} & Exec = 0.587 \end{array}$$

APPENDIX K

APPENDIX K - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER - COUPLED INDUCTOR 50 KHZ

Projeto Físico do Indutor Lm - Conversor CC-CA Flyback com GA

1.Especificações:

Indutância	L _{mp} := 26.062µH
Valor máximo de corrente	I _{Lnuico} := 47.619A
Valor eficaz de corrente no primário	I _{prief} := 21.497A
Valor eficaz de corrente no primário (cc)	Ipriefic := 0A
Valor eficaz de corrente no primário (ca)	I _{priefca} := 21.497A
Valor eficaz de corrente no secundário	$I_{secef} := 4.009 A$
Valor eficaz de corrente no secundário (cc)	$I_{secefcc} := 0 A.$
Valor eficaz de corrente no secundário (ca)	$I_{secefca} := 4.009 A$
Ondulação de Corrente	$\Delta I_{Lm} := 19.048 A$
Relação de Transformação	a := 4.276
Fluxo de indução máximo	B _{max} := 0.33T
Densidade máxima de corrente	$J_{\max} := 420 \frac{A}{cm^2}$ $k_w := 0.7$
Fator de utilização da área do núcleo	$\mathbf{k}_{\mathbf{W}} \coloneqq 0.7$
Frequência de Comutação	$\mathbf{f}_{s} := 50 \mathrm{kHz}$
2. Escolha do Núcleo:	
$AeA_{W} := \frac{L_{mp} \cdot I_{Lmpico} \cdot \left(I_{prief} + 2a \cdot I_{secef}\right)}{B_{max} \cdot J_{max} \cdot k_{w}}$	$AeAw = 7.135 \cdot cm^4$
Núcleo Escolhido: E65/32/27 3C90	$A_e := 5.4 \text{ cm}^2$ $A_w := 3.94 \text{ cm}^2$ $I_c := 4.44 \text{ cm}$
3. Cálculo do Número de Espiras:	
$N_{\text{pri}} \coloneqq \text{ceil} \left(\frac{L_{\text{mp}} \cdot I_{\text{Lmpico}}}{B_{\text{max}} \cdot A_{\text{e}}} \right)$	N _{pri} = 7
$B_{\text{max}} = \frac{L_{\text{mp}} \cdot I_{\text{Lmpico}}}{N_{\text{pri}} \cdot A_{e}}$	$\mathbf{B}_{\max} = 0.328 \cdot \mathbf{T}$

N_{sec} = 30

4. Cálculo do entreferro:

$$l_{entreferro} := \frac{N_{pri}^2 \cdot \mu_0 \cdot A_e \cdot \left(10^{-2} \cdot \frac{m}{cm}\right)}{L_{mm}}$$

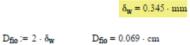
l_{entreferro} = 1.276 · mm

5. Cálculo da bitola do condutor:

 $T_{max} := 100$ $\eta_{W} := 0.8$..-9 r.

$$\rho_{T} := 17.9 \cdot 10^{-9} \cdot [1 + 0.0039(T_{max} - 20)] \cdot \Omega \cdot m$$

$$\delta_{\mathbf{w}} := \sqrt{\frac{\rho_{\mathbf{T}}}{\pi \cdot \mu_0 \cdot \mathbf{f}_s}}$$



O condutor escolhido é o 38AWG.

dw := 0.10mm

 $S_{fio} := 0.000080 \cdot cm^2$

 $S_{cobrepri} := \frac{I_{prief}}{J_{max}}$

$$\begin{split} \mathbf{n}_{condpri} &\coloneqq \operatorname{ceil}\!\left(\frac{S_{cobrepri}}{S_{\mathrm{fio}}}\right) \\ \mathbf{x} &\coloneqq \operatorname{ceil}\!\left(\frac{\mathbf{n}_{condpri}}{41}\right) \end{split}$$

Acondprix = 41 · x

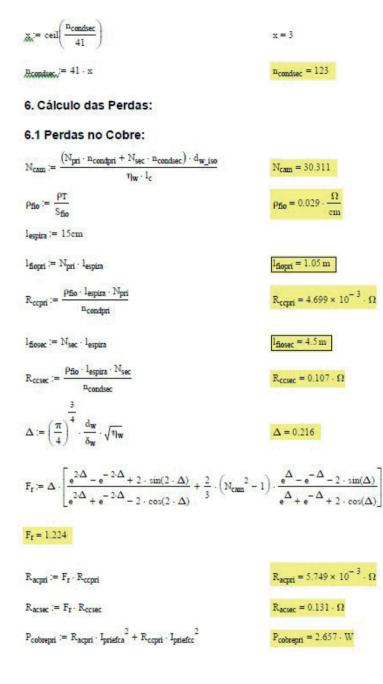
 $S_{cobresec} := \frac{I_{secef}}{J_{max}}$

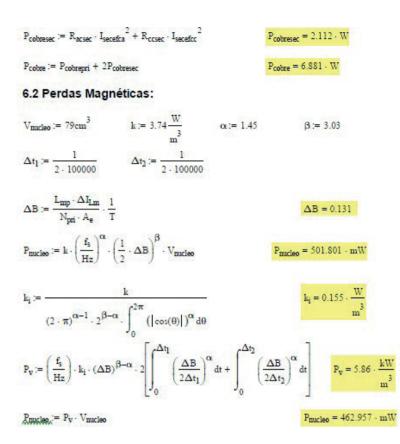
 $n_{\text{condsec}} := \text{ceil}\left(\frac{S_{\text{cobresec}}}{S_{\text{fio}}}\right)$

dw_iso := 0.13mm $S_{fioiso} := 0.000130 \cdot cm^2$ $S_{cobrepri} = 0.051 \cdot cm^2$ n_{condpri} = 640 x = 16 n_{condpri} = 656

$$S_{cobresec} = 9.545 \times 10^{-3} \cdot cm^2$$

 $n_{condsec} = 120$





6.3 Perdas Totais:

Ptotais := Pcobre + Pnucleo

P_{totais} = 7.344 · W

6.4 Resistência Térmica do Núcleo:

$Rt_{micleo} := 23 \cdot \frac{K}{W}$	$\left(\frac{A_e A_w}{4}\right)^{-0.37}$	$Rt_{\text{funcleo}} = 7.42 \cdot \frac{K}{W}$
	(CIII)	

6.5 Elevação de Temperatura:

 $\Delta T = 54.492 \text{ K}$

7. Possibilidade de Execução:

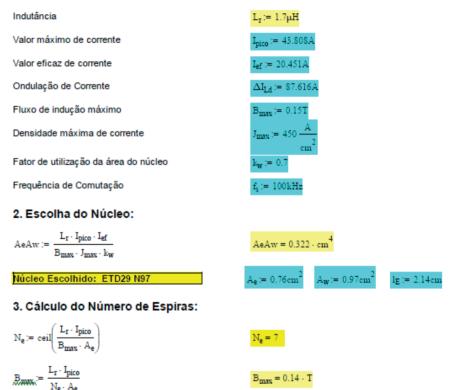
$$\begin{split} A_{\mathbf{w_min}} &\coloneqq \frac{N_{\mathbf{pri}} \cdot S_{\mathbf{fioiso}} \cdot \mathbf{n_{condpri}} + 2N_{\mathbf{sec}} \cdot S_{\mathbf{fioiso}} \cdot \mathbf{n_{condsec}}}{k_{\mathbf{w}}} \qquad A_{\mathbf{w_min}} = 2.223 \cdot \mathrm{cm}^2 \\ E_{\mathrm{xec}} &\coloneqq \frac{A_{\mathbf{w_min}}}{A_{\mathbf{w}}} \qquad \qquad \underbrace{E_{\mathrm{xec}} = 0.564} \end{split}$$

APPENDIX L

APPENDIX L - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER – AUXILIARY SWITCHING INDUCTOR 100 KHZ

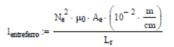
Projeto Físico do Indutor L_d - Conversor Boost-Flyback

1.Especificações:



l_{entreferro} = 2.753 - mm

4. Cálculo do entreferro:



5. Cálculo da bitola do condutor:

T_{max} := 100

 $\eta_{w} := 0.8$

$$\begin{split} \rho_{\mathrm{T}} &\coloneqq 17.9 \cdot 10^{-9} \cdot \left[1 + 0.0039 (\mathrm{T}_{\mathrm{max}} - 20) \right] \cdot \Omega \cdot \mathrm{m} \\ \delta_{\mathrm{W}} &\coloneqq \sqrt{\frac{\rho_{\mathrm{T}}}{\pi \cdot \mu_{0} \cdot \mathrm{f}_{\mathrm{s}}}} & \delta_{\mathrm{W}} = 0.244 \cdot \mathrm{mm} \\ \mathrm{Di}_{\mathrm{fin}} &\coloneqq 0.1000 \mathrm{Fio} : D_{\mathrm{fio}} &\coloneqq 2 \cdot \delta_{\mathrm{W}} & D_{\mathrm{fio}} = 0.049 \cdot \mathrm{cm} \\ \mathrm{D}_{\mathrm{condutor}} & \mathrm{escolhido} \stackrel{e}{\bullet} o \, 38A\mathrm{WG.} \\ \mathrm{d}_{\mathrm{W}} &\coloneqq 0.1\mathrm{mm} & \mathrm{d}_{\mathrm{W}_{\mathrm{s}}\mathrm{iso}} &\coloneqq 0.13\mathrm{mm} \\ \mathrm{S}_{\mathrm{fio}} &\coloneqq 0.000080 \cdot \mathrm{cm}^{2} & \mathrm{S}_{\mathrm{fotso}} &\coloneqq 0.000130 \cdot \mathrm{cm}^{2} \\ \mathrm{S}_{\mathrm{cobre}} &\coloneqq \frac{\mathrm{I}_{\mathrm{ef}}}{\mathrm{J}_{\mathrm{max}}} & \mathrm{S}_{\mathrm{cobre}} &= 0.045 \cdot \mathrm{cm}^{2} \\ \mathrm{n}_{\mathrm{cond}} &\coloneqq \mathrm{ceil} \left(\frac{\mathrm{S}_{\mathrm{cobre}}}{\mathrm{S}_{\mathrm{fio}}} \right) & \mathrm{n}_{\mathrm{litz}} &= 14 \end{split}$$

Acond, = 41 · nlitz

6. Cálculo das Perdas:

6.1 Perdas no Cobre:

$$\begin{split} N_{cam} &\coloneqq \frac{N_{e} \cdot n_{cond} \cdot d_{w_{i}iso}}{\eta_{w} \cdot l_{E}} \\ \rho_{fio} &\coloneqq \frac{\rho_{T}}{S_{fio}} \\ l_{espira} &\coloneqq 5.28 \, \mathrm{cm} \end{split}$$

 $l_{fio} := N_e \cdot l_{espira}$

$$\begin{split} \mathbf{R}_{\mathsf{cc}} &\coloneqq \frac{\rho_{\mathsf{fio}} \cdot \mathbf{l}_{\mathsf{espira}} \cdot \mathbf{N}_{\mathsf{e}}}{n_{\mathsf{cond}}} \\ \Delta &\coloneqq \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \cdot \frac{\mathbf{d}_{\mathsf{w}}}{\delta_{\mathsf{w}}} \cdot \sqrt{\eta_{\mathsf{w}}} \end{split}$$

 $n_{cond} = 574$

$$R_{cc} = 1.89 \times 10^{-3} \cdot \Omega$$

 $\Delta = 0.306$

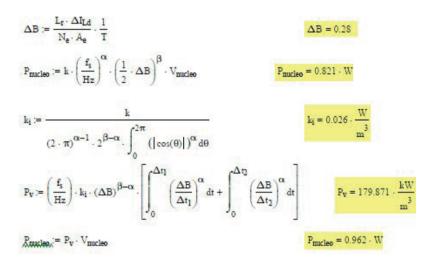
$$F_{\mathbf{r}} \coloneqq \Delta \cdot \left[\frac{e^{2\boldsymbol{\Delta}} - e^{-|\boldsymbol{\Delta}|} + 2 \cdot \sin(2 \cdot \boldsymbol{\Delta})}{e^{2\boldsymbol{\Delta}} + e^{-|\boldsymbol{\Delta}|} - 2 \cdot \cos(2 \cdot \boldsymbol{\Delta})} + \frac{2}{3} \cdot \left(N_{cam}^2 - 1 \right) \cdot \frac{e^{\boldsymbol{\Delta}} - e^{-|\boldsymbol{\Delta}|} - 2 \cdot \sin(\boldsymbol{\Delta})}{e^{\boldsymbol{\Delta}} + e^{-|\boldsymbol{\Delta}|} + 2 \cdot \cos(\boldsymbol{\Delta})} \right]$$

$$F_{I} = 1.906$$

$$R_{ac} := F_r \cdot R_{cc} \qquad \qquad R_{ac} = 3.602 \times 10^{-3} \cdot \Omega$$
$$P_{cobre} := R_{ac} \cdot I_{ef}^{-2} \qquad \qquad P_{cobre} = 1.507 \cdot W$$

6.2 Perdas Magnéticas:

 $V_{\text{nucleo}} := 5.35 \text{cm}^3 \qquad \text{k} := 0.478 \frac{\text{W}}{\text{m}^3} \qquad \alpha := 1.53 \qquad \beta := 2.51$ $\Delta t_1 := 7.38 \times 10^{-6} \qquad \Delta t_2 := 1.702 \times 10^{-6}$



6.3 Perdas Totais:

 $P_{totais} = 2.469 \cdot W$

6.4 Resistência Térmica do Núcleo:

$$Rt_{mcleo} \coloneqq 23 \cdot \frac{K}{W} \left(\frac{A_e A_w}{cm^4} \right)^{-0.37} Rt_{mcleo} = 25.747 \cdot \frac{K}{W}$$

6.5 Elevação de Temperatura:

 $\Delta T := (P_{cobre} + P_{nucleo})Rt_{nucleo}$

7. Possibilidade de Execução:

$$A_{w_min} := \frac{N_{e} \cdot S_{fioiso} \cdot n_{cond}}{k_{w}} \qquad \qquad A_{w_min} = 0.746 \cdot cm^{2}$$

$$Exec := \frac{A_{w_min}}{A_{w}} \qquad \qquad Exec = 0.769$$

 $\Delta T = 63.567 \, \mathrm{K}$

APPENDIX M

APPENDIX M - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER – AUXILIARY SWITCHING INDUCTOR 50 KHZ

Projeto Físico do Indutor L_d - Conversor Boost-Flyback

1.Especificações:	
Indutância	L ₁ := 3.5µH
Valor máximo de corrente	I _{pico} := 47.619A
Valor eficaz de corrente	$I_{ef} := 21.497 A$
Ondulação de Corrente	ΔI _{Ld} := 95.238A
Fluxo de indução máximo	B _{max} := 0.3T
Densidade máxima de corrente	$J_{max} := 550 \frac{A}{cm^2}$
Fator de utilização da área do núcleo	$\mathbf{k}_{w} := 0.7$
Frequência de Comutação	$f_s := 50 kHz$
2. Escolha do Núcleo:	
$AeAw := \frac{L_{\tau} \cdot I_{pico} \cdot I_{ef}}{B_{max} \cdot J_{max} \cdot k_{w}}$	AeAw = 0.31 · cm ⁴
Núcleo Escolhido: ETD29 N97	$A_e := 0.76 \text{cm}^2$ $A_w := 0.97 \text{cm}^2$ $l_E := 2.14 \text{cm}$
3. Cálculo do Número de Espiras:	
$N_e := ceil \left(\frac{L_r \cdot I_{pico}}{B_{max} \cdot A_e} \right)$	N _c = 8
$\underset{N_{e} \in A_{e}}{\underset{N_{e} \in A_{e}}{\underbrace{L_{r} \cdot I_{pico}}}}$	$B_{max} = 0.274 \cdot T$
4. Cálculo do entreferro:	
N^2 , μ_0 , $A_{10} \left(10^{-2}, \frac{m}{m} \right)$	

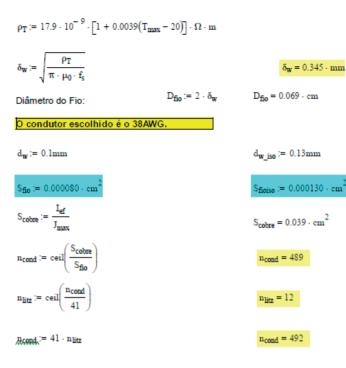
l_{entreferro} = 1.746 · mm

 $l_{entreferro} := \frac{N_e^{-2} \cdot \mu_0 \cdot A_e \cdot \left(10^{-2} \cdot \frac{m}{cm}\right)}{L_r}$

5. Cálculo da bitola do condutor:

T_{max} := 100

η_w := 0.8



6. Cálculo das Perdas:

6.1 Perdas no Cobre:

$$\begin{split} N_{cam} &:= \frac{N_{e} \cdot n_{cond} \cdot d_{w_{a}iso}}{\eta_{w} \cdot i_{E}} & N_{cam} = 29.888 \\ \rho_{fio} &:= \frac{\rho_{T}}{S_{fio}} & \rho_{fio} = 0.029 \cdot \frac{\Omega}{cm} \\ l_{espira} &:= 5.28 cm \\ l_{fio} &:= N_{e} \cdot l_{espira} & l_{fio} = 0.422 m \\ R_{cc} &:= \frac{\rho_{fio} \cdot l_{espira} \cdot N_{e}}{n_{cond}} & R_{cc} = 2.52 \times 10^{-3} \cdot \Omega \\ \Delta &:= \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \cdot \frac{d_{w}}{\delta_{w}} \cdot \sqrt{\eta_{w}} & \Delta = 0.216 \end{split}$$

$$\mathbf{F}_{\mathbf{f}} \coloneqq \Delta \cdot \left[\frac{e^{2\cdot\Delta} - e^{-2\cdot\Delta} + 2\cdot\sin(2\cdot\Delta)}{e^{2\cdot\Delta} + e^{-2\cdot\Delta} - 2\cdot\cos(2\cdot\Delta)} + \frac{2}{3}\cdot \left(N_{cam}^2 - 1 \right) \cdot \frac{e^{\Delta} - e^{-\Delta} - 2\cdot\sin(\Delta)}{e^{\Delta} + e^{-\Delta} + 2\cdot\cos(\Delta)} \right]$$

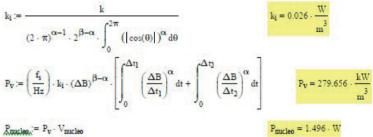
F_r = 1.217

$$R_{ac} := F_{r} \cdot R_{cc} \qquad \qquad R_{ac} = 3.068 \times 10^{-3} \cdot \Omega$$

$$P_{cobre} := R_{ac} \cdot I_{ef}^{2} \qquad \qquad P_{cobre} = 1.418 \cdot W$$

6.2 Perdas Magnéticas:

$$\begin{split} \mathrm{V}_{\text{nucleo}} &\coloneqq 5.35 \text{cm}^3 \qquad \mathrm{k} \coloneqq 0.478 \frac{\mathrm{W}}{\mathrm{m}^3} \qquad \alpha \coloneqq 1.53 \qquad \beta \coloneqq 2.51 \\ \Delta t_1 &\coloneqq 14 \times 10^{-6} \qquad \Delta t_2 \coloneqq 6 \times 10^{-6} \\ \Delta B &\coloneqq \frac{\mathrm{L}_{\mathrm{f}} \cdot \Delta \mathrm{I}_{\mathrm{Ld}}}{\mathrm{N}_{\mathrm{e}} \cdot \mathrm{A}_{\mathrm{e}}} \cdot \frac{1}{\mathrm{T}} \qquad \Delta B = 0.548 \\ \mathrm{P}_{\text{nucleo}} &\coloneqq \mathrm{k} \cdot \left(\frac{\mathrm{f}_{\mathrm{s}}}{\mathrm{Hz}}\right)^{\alpha} \cdot \left(\frac{1}{2} \cdot \Delta B\right)^{\beta} \cdot \mathrm{V}_{\text{nucleo}} \qquad \mathrm{P}_{\text{nucleo}} = 1.536 \cdot \mathrm{W} \end{split}$$



6.3 Perdas Totais:

Ptotais := Pcobre + Pnucleo

 $P_{totais} = 2.914 \cdot W$

6.4 Resistência Térmica do Núcleo:

$$Rt_{mucleo} := 23 \cdot \frac{K}{W} \left(\frac{A_e A_w}{cm^4} \right)^{-0.37} \qquad Rt_{mucleo} = 25.747 \cdot \frac{K}{W}$$

6.5 Elevação de Temperatura:

 $\Delta T := (P_{cobre} + P_{nucleo})Rt_{nucleo}$

ΔT = 75.026 K

7. Possibilidade de Execução:

 $A_{w_min} := \frac{N_{e} \cdot S_{fioiso} \cdot n_{cond}}{k_{w}}$

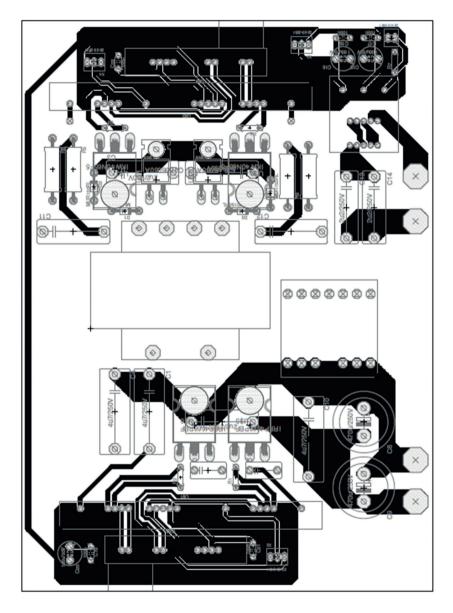
 $A_{w \min} = 0.731 \cdot cm^2$

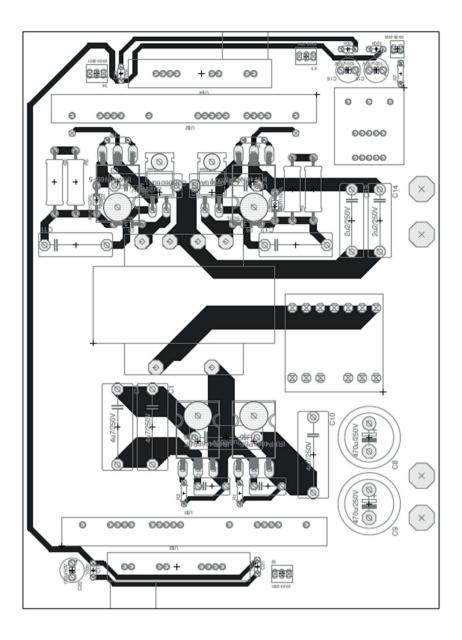
 $Exec := \frac{A_{w_min}}{A_w}$

Exec = 0.754

APPENDIX N

APPENDIX N - DC-AC ACTIVE-CLAMPING FLYBACK CONVERTER - PCB LAYOUT





ANALYSIS, DESIGN AND IMPLEMENTATION OF SINGLE-STAGE HIGH-FREQUENCY-ISOLATED DC-AC FLYBACK CONVERTERS

- www.atenaeditora.com.br
- 🔀 contato@atenaeditora.com.br
- @atenaeditora
 - www.facebook.com/atenaeditora.com.br



ANALYSIS, DESIGN AND IMPLEMENTATION OF SINGLE-STAGE HIGH-FREQUENCY-ISOLATED DC-AC FLYBACK CONVERTERS

- www.atenaeditora.com.br
- 🔀 contato@atenaeditora.com.br
- @ atenaeditora
 - www.facebook.com/atenaeditora.com.br

