v. 2, n. 25, 2022

Journal of
Engineering
Research

SINGLE-DC-SOURCE QUASI-Z-SOURCE CASCADED MULTILEVEL INVERTER WITH ACTIVE POWER SHARING

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Abstract: This paper proposes a novel cascaded multilevel topology, named Single-dc-Source quasi-Z Source Cascade Multilevel Inverter. This inverter has the ability to provide independent regulation of the dc bus voltage of each H-bridge, ensuring real power balancing and true symmetric to the multilevel waveforms. In addition, the Single-dc-Source quasi-Z Source Cascade Multilevel Inverter allows operating with a single low power PV array. This paper provides a detailed analysis of operation with a design methodology for the hardware, as well as modeling and controller design. Simulation results are provided to verify the proposed system operation and control strategy.
Keywords: Cascaded, LCL filter, Quasi-Z Source inverter.

INTRODUCTION

Owing to the decentralized MPPT and multilevel output voltage waveform, the cascade multilevel inverter (CMI) is often regarded as one of the most attractive PV inverter topologies, holding advantages such as better immunity for shadowing and mismatching issues, smaller sized filter components, reduced switching frequency and losses, low harmonic distortion of the generated output voltage, high efficiency, and so on (Rodríguez *et al.*, 2007). Nonetheless, since the lack of boost function of the conventional CMI, the distributed MPPT may lead to different maximum power points of the separate PV panels, yielding in inherent voltage and power imbalance within the CMI. The mismatched dc bus voltage may introduce distortions in the injected grid current. To overwhelm such limitations, two alternatives have been presented separately in the literature, consisting in (i) the use of single dc source CMI (Du *et al.*, 2006); and (ii) the employment of quasi-Z-source cascaded multilevel inverter (qZS-CMI) (Liu, Ge and Abu-rub, 2014). In the former approach, only one H-bridge cell is supplied by a real dc power source, meanwhile the remaining cells are supplied by capacitors (Sepahvand *et al.*, 2013). In such topologies, the control method provides capacitor voltage regulation for each H-bridge cell and thus, avoiding the abovementioned distortions. Furthermore, since adequate multilevel output voltage waveform is achieved, it attains low harmonic distortion of the generated output voltage and to reduce the switching frequency of the CMI. Nonetheless, only the dc power sourced H-bridge cell can sustain real power to the load. This limitation avoids the power sharing among the H-bridge cells; and hence, only the dc power source bridge withstands the total real power of the CMI.

On the other way, the later approach presents in its structure a merged boost function achieved by its shoot-through state, which adds an extra degree of freedom to the qZS-CMI control. Nevertheless multiple independent real dc power sources are required. Thus, real power sharing is achieved by the expense of providing an independent PV array for each CMI H-bridge, which in turn requires a large amount of installed PV power.

In order to provide a solution that ensure the advantages of the qZS-CMI employing a single low power string PV array the Single dc Source quasi-Z Source Cascade Multilevel Inverter (SS qZS-CMI) is proposed. Fig. 1 shows the diagram of the proposed inverter. It provides MPPT for the single PV array and dc bus voltage regulation for each H-bridge cell. It also can share active power between the H-bridges by means of the power transfer through a transformer/coupled inductor component. This feature permits a better utilization of the H-bridge devices, such as the dc bus inductors and capacitors as well as the semiconductor devices.

DESCRIPTION OF SS QZS-CM INVERTER

Fig. 1 shows a SS qZS-CMI grid-tie PV power system. In its simplest form it consists of two qZ-source H-bridge cells. The main bridge is fed by a five PV array, of the company Sunmodule, model SW 285-300. Whose characteristics are, maximum power (P_{max}) 285 Wp, open circuit voltage (V_{oc}) 39.7 V, maximum power point voltage (V_{mpp}) 31.3 V, short circuit current (I_{sc}) 9.84 A and maximum power point current (I_{mpp}) 9.2 A. That characterizes the topology as a single dc source inverter. The auxiliary bridge presents a capacitor that plays the role of input voltage source. This capacitor is charged solely by the secondary winding of a coupled-inductor whose primary winding is magnetized by the main H-bridge module during its shoot-through state. This unique feature allows both active and reactive power to be processed by the auxiliary H-bridge cell.

The total output voltage of the inverter is a series sum of SS qZS-HBI module voltages. The dc bus voltage of each module is controlled independently, which ensures that the dc bus voltage ratio is kept constant. This characteristic is essential to enable the topology to work such as a symmetric multilevel inverter, holding its advantages.

For the system's modulation, the PS-SPWM method in (Sun *et al.*, 2012) is employed, and the carriers of the two modules are shifted by 180º to each other. As a result, the SS qZS-CMI provides a five-level output voltage v_H to feed the 60-Hz grid through the LCL-filter.

SS QZS-CMI OPERATING PRINCIPLE

Taking into account a single qZ-source H-bridge cell, it can be state that its operation consists in two distinct operating states (Ge *et al.*, 2013), the non-shoot-through and shoot-through states. At the non-shoot-through state, the power is transmitted from the dc side to the ac side for each qZ-source H-bridge cell. On the other hand, at the shoot-through state, there is no power transmission from dc through ac in each bridge, because the dc-link voltage is zero. Nevertheless, during the shoot-through state, main H-bridge coupled inductor energy is transferred from its primary winding to its secondary winding, charging the input capacitor of the auxiliary qZ-source H-bridge cell, as we can see in Fig. 2(a) and Fig. 2(b).

SYSTEM MODELING AND CONTROL

PV VOLTAGE LOOP (MPPT)

The PV voltage control block diagram of the main module is shown in Fig. 3(a), where the transfer function of the input voltage by the shoot-through duty ratio is given by,

$$G_{I_{PN}}^{V_{PN(a)}}(s) = \frac{V_{in}}{D_0}(s) = \frac{-C_{Bus}\left(V_{C1}+V_{C2}\right)s + \left(I^* - 2D_{0(a)}I^*\right)}{C_{in}C_{Bus}L_{Bus}s^3 + 4C_{in}\left(D_{0(a)}-0.5\right)^2 s} \quad (1)$$

where $I^* = I_{Load} - I_{L1} - I_{L2}$.

The voltage controller applied to (1) is a PI regulator represented by the block ($C_1(s)$). Its transfer function is

$$G_{Pi}(s) = K_p\left(s + \frac{K_i}{K_p}\right)\Big/ s \quad (2)$$

Since the maximum power point tracking dynamics is very slow, the design of the PI parameters yields a bandwidth of 3.02 Hz with a phase margin of 40.2°.

MAIN H-BRIDGE DC-BUS VOLTAGE CONTROL (REF. IG)

The independent dc-bus peak voltage ($V_{PN(a)}$) control based on the capacitors voltage summation ($V_{C1} + V_{C2}$) is performed for the main H-bridge, as Fig. 3(b) shows.

The transfer function of the bus voltage V_{PN} by the H-bridge current (I_{PN}), defined as $G_{I_{PN}}^{V_{PN(a)}}(s)$, is,

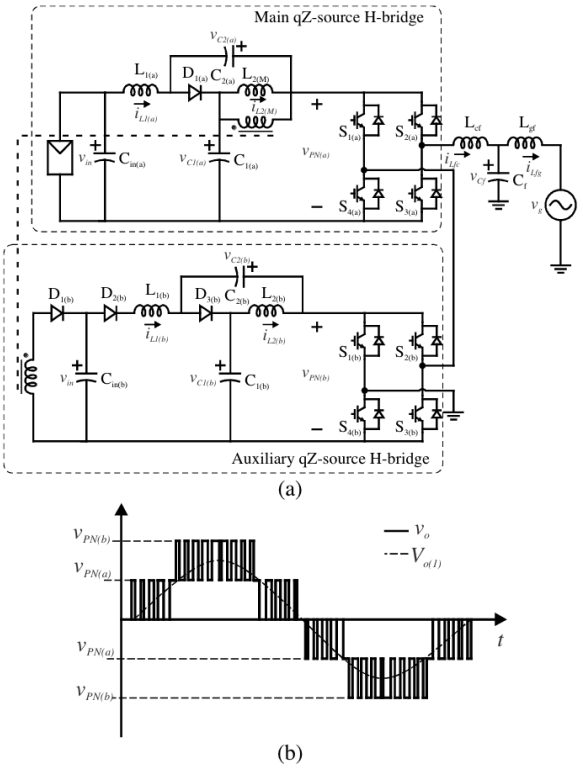


Fig. 1 - Single-DC-Source 5-level Symmetric qZS-CMI based PV system. (a) Circuit diagram and (b) Key waveforms.

$$G_{I_{PN}}^{V_{PN(a)}}(s)=\frac{V_{PN(a)}}{I_{PN}}(s)=\frac{-L_{Bus}\left(1-D_{0(a)}\right)s}{C_{Bus}L_{Bus}s^2+\left(D_{0(a)}-0.5\right)^2} \quad (3)$$

The voltage controller applied to (3) is also a PI regulator.

Since the controller output provides reference for the inner current loop, it is design to provide lower bandwidth than the current control loop, nevertheless, as long as the capacitors $C_{1(a)}$ and $C_{2(a)}$ are fed by the input voltage dynamic, the controller must yield fast response to V_{PN} when compared to V_{in}. This way, the PI controller had been designed to provide a 33.2 Hz bandwidth with a 107° of phase margin.

GRID-TIE CURRENT LOOP

The transfer function of the grid-injected current can be given by,

$$G_{m_a}^{i_{Lg}}(s)=\frac{i_{Lg}(s)}{m_a(s)}=\frac{1}{C_f L_f L_g}\frac{V_{PN}}{s^3+\omega_1^2 s} \quad (4)$$

where the resonant frequency is $\omega_1=\sqrt{\left(L_f+L_g\right)/C_f L_f L_g}$.

This third order system is referred as $G_{m_a}^{i_{Lg}}(s)$.

In Fig. 3(c) the grid-tie dual-loop current control is shown. It can be seen that an outer voltage loop provides the grid current reference I_g^*, which means that the regulator's output of the dc bus voltage control loop ($C_2(s)$) multiplied by a sinusoidal function synchronized to the grid's phase voltage by a phase locked loop, yields in the instantaneous phase current reference. The P+resonant compensator ($C_{Res}(s)$) (Timbus *et al.*, 2009) is used, as long as typical PI regulator performance would be poor with low phase margin.

In addition to the abovementioned dual-loop control, an extra control loop is used exclusively to implement active damping to the system (Tang et al., 2012). The active damping avoids the natural resonance problems of the LCL without penalizing system efficiency and for this application requires the measurement of the filter capacitor current.

In order to design the P+resonant controller constants it is required to know the transfer function of the grid current by the modulation index given by expression (4).

The transfer function of the P+resonant controller is given by (5). It allows tracking sinusoidal references with null steady-state error.

$$G_{PR}(s)=k_{iP}+\frac{k_{iR}\omega_0}{s^2+\omega_0^2} \quad (5)$$

The resonance frequency for the P+resonant controller is defined by (6).

$$10\omega_g \le \omega_{res} \le 0.5\omega_s \quad (6)$$

The PR controller with active damping provided a bandwidth of 1000 Hz with a phase margin of 46.3°.

AUXILIARY H-BRIDGE DC-BUS VOLTAGE CONTROL (SHOOT-T)

The auxiliary H-bridge input voltage is defined by the shoot-through ratio and the turns ratio of the coupled inductor N. Hence, in order to control the dc-Bus voltage of the auxiliary H-bridge, the available control variable is its shoot-through duty ratio.

The independent dc-bus peak voltage ($V_{PN(a)}$) control based on the capacitors voltage summation (V_{C1} +V_{C2}) is performed for the main H-bridge, as Fig. 3(b) shows.

The transfer function of the bus voltage $V_{PN(b)}$ by the shoot-through ratio ($D_{0(b)}$), defined as $G_{D_{0(b)}}^{V_{PN(b)}}(s)$,

$$G_{D_{0(b)}}^{V_{PN(b)}}(s) = \frac{V_{PN(b)}(s)}{D_{0(b)}(s)} = \frac{I^* L_{Bus} s + \left[V_{C1}\left(1-2D_{0(b)}\right)+V_{C2}\left(1-2D_{0(b)}\right)\right]}{C_{Bus} L_{Bus} s^2 + \left(D_{0(b)}-0.5\right)^2} \quad (7)$$

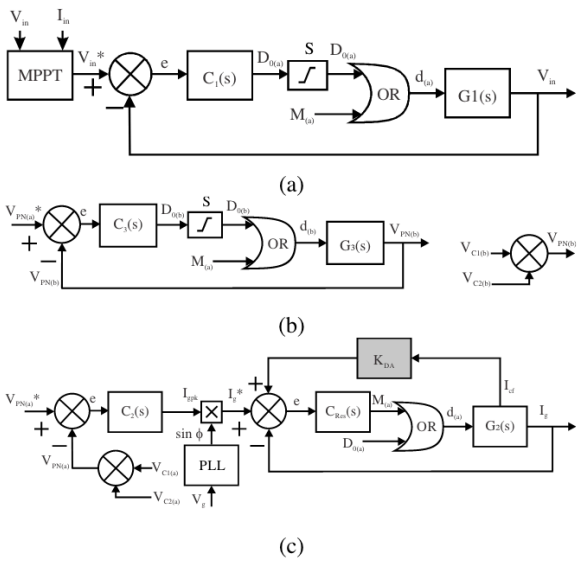


Fig. 3. Block diagram of the Single-DC-Source 5-level qZS-CMI control loops. (a) V_{in} control loop; (b) Independent DC-bus voltage $V_{PN(b)}$ control loop; (c) Grid-tie current control.

The voltage controller applied to (7) is a PI regulator designed to provide a bandwidth of 12.1 Hz with a phase margin of 95.6°.

Fig. 4 shows block diagram of the overall proposed grid-tie control with the system model for the qZS-CMI based PV power system.

SS QZS-CMI-BASED GRID-TIE PV INVERTER PARAMETER DESIGN

Z-IMPEDANCE PARAMETERS DESIGN

In shoot-through state, the two qZS inductors L_1 and L_2 magnetize and the voltages across them are equal to the voltage v_{C1}. This way, to limit the high-frequency ripple of such inductors and also to ensure the operation under continuous conduction current mode (CCM), the impedance inductances for the main H-bridge are given by,

$$L_{1(a)} \geq \frac{V_{C1(a)} D_{0(a)Max}}{2\Delta I_{L1(a)} f_s};\ L_{2(a)} = \frac{V_{C2(a)} D_{0(a)}}{2\Delta I_{L2(a)}(t) f_s} \quad (8)$$

where $D_{0(a,b)Max} = 1\text{-}M_{min}$.

Analogously, the auxiliary H-bridge impedance inductances are defined by (9).

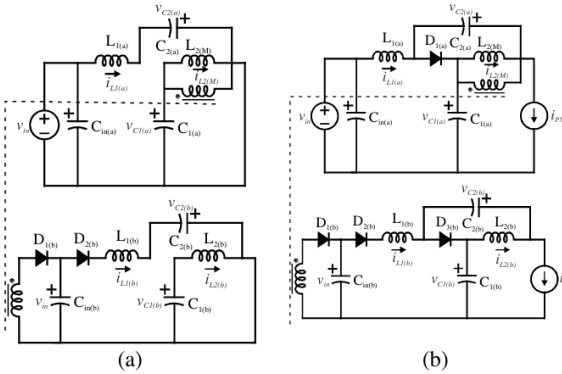


Fig. 2-Single-DC-Source 5-level qZS-CMI operating states. (a) shoot-through state; (b) non shoot-through state.

$$L_{1(b)} \geq \frac{V_{C1(b)} D_{0(b)Max}}{2\Delta I_{L1(b)} f_s};\ L_{2(b)} = \frac{V_{C2(b)} D_{0(b)}}{2\Delta I_{L2(b)}(t) f_s} \quad (9)$$

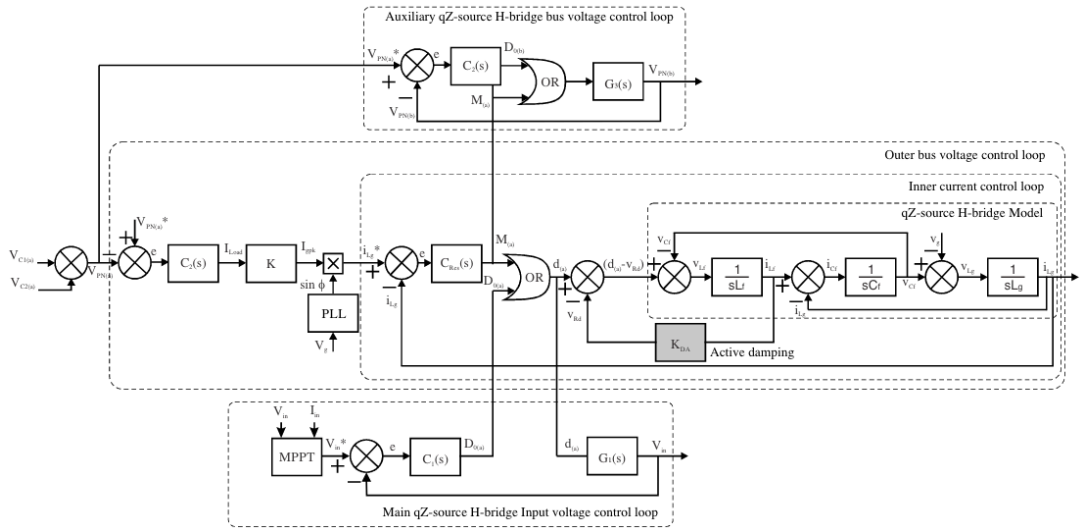


Fig. 4. Block diagram of the proposed grid-tie control with the model for the qZS-CMI based PV system.

On the contrary, in non-shoot-through state, the impedance capacitors are in series. Thus, to limit the voltage ripple on the H-bridge to a certain value the capacitances should be defined by

$$C_{1(a)} = C_{2(a)} = \frac{P_{out}}{\pi f_{ripple} \Delta V_{bus}(\%) V_{Cout}}; \quad C_{1(b)} = C_{2(b)} = \frac{P_{out}}{\pi f_{ripple} \Delta V_{bus}(\%) V_{Cout}}. \tag{10}$$

The design of the turns ratio of the coupled inductor can be given by (11), where $V_{PN(a)}/V_{PN(b)}$ is equal the unity.

$$N = \frac{1-2D_{0(a)}}{\left(V_{PN(a)}/V_{PN(b)}\right)\left(1-D_{0(a)}\right)} \tag{11}$$

LCL FILTER DESIGN

The design of the LCL filter is based on the power rating of the converter, the line and the switching frequencies. Normally, the filter values are reported as a percentage of the base values (Twining and Holmes, 2003), given by,

$$Z_b = \frac{V_{g(RMS)}^2}{P_o}; \quad C_b = \frac{1}{\omega_n Z_b} \tag{12}$$

where V_g is the line RMS voltage, ω_n is the grid frequency, and P_o is the active power absorbed by the converter in rated conditions.

The resonant frequency is referred to the switching frequency value by $\omega_n = k\omega_s$, where *k* expresses how far the switching frequency is from the resonant frequency of the filter. The resonant frequency range usually is defined as

$$10\omega_g < \omega_n < 0.5\left(2\pi f_s\right) \tag{13}$$

where the resonant frequency is given by,

$$\omega_n = \sqrt{\left(L_f + L_g\right)/L_f L_g C_f} \tag{14}$$

The maximum current ripple at the output of dc/ac inverter happens for the modulation index equal 0.5 and is given by:

$$\Delta_{IL} = \frac{2V_{PN}}{3L_f f_s}(1-m)m \therefore \Delta_{IL(Max)}\Big|_{m=0.5} = \frac{V_{PN}}{6 f_s L_f} \tag{15}$$

Hence, the inverter side inductor (L_f) can be calculated as,

$$L_f = \frac{V_{PN}}{6 f_s \Delta_{IL(Max)}} \approx \frac{V_{PN}}{0.6 f_s I_{PN}} \tag{16}$$

The ripple attenuation, passing from the converter side to the grid side, can be calculated as,

$$\frac{I_g(h)}{I_i(h)} = \frac{1}{\left[1 + r\left(1 - L_g C_b \omega_s^2 x\right)\right]} = k_a \quad (17)$$

or

$$L_g = \left(\sqrt{\frac{1}{k_a^2}} + 1\right) \Big/ \left(C_f \omega_s^2\right) \quad (18)$$

Where k_a is the desired attenuation and C_f = 0.01/0.05C_b. In Table I we can see the parameters used in the simulation.

The constant r is the ratio between the inductance at the inverter side (L_f) and the one at the grid side (L_g). Thus, $L_g = rL_f$.

Parameters	Specification	Values
C_1, C_2	Input network capacitor	4.7 mF
C_f	Filter capacitor	4.242 uF
$D_{0(a)}$, $D_{0(b)}$	ST maximum duty cycle	0.4
I_{PN}	DC bus current	6.81 A
$\Delta I_{L1(a)}, \Delta I_{L2(a)}$	Project choice	10 %
$\Delta I_{L1(b)}, \Delta I_{L2(b)}$	Project choice	10 %
ΔV_{bus}	Project choice	22.5 %
L_1, L_2	Input network inductor	2.568 mH
L_f	Converter side inductor	1.750 mH
L_g	Grid side inductor	0.860 mH
$V_{in(a)}$, $V_{in(b)}$	Input voltage	155 V
$V_{g(rms)}$	Grid voltage rms	220 V
f_g	Grid frequency	60 Hz
f_s	Switching frequency	10.02 kHz
P_n	Output power	1.5 kW
$V_{PN(a)}$, $V_{PN(b)}$	DC bus voltage	259 V
f_{res}	Resonance frequency	3.4 kHz
K_{PWM}	Modulator gain	0.5

Table 1-Specifications SS qZS-CMI.

For passive damping, usually a resistor in series (R_f) with the capacitor attenuates part of the ripple on the switching frequency in order to avoid the resonance.

$$R_f = \frac{1}{3\omega_{res} C_f} \quad (19)$$

ACTIVE DAMPING DESIGN

Aiming to provide the active damping (Liserre, Blaabjerg and Hansen, 2005) for the LCL filter, it is required to include an additional control loop to the system. The addition to this extra control loop results in the following transfer function.

$$G_{Pd}(s) = \frac{2V_{PN}K_{PWM}}{s(C_f L_f L_g s^2 + 2V_{PN}K_{PWM}K_{DA}C_f L_g s + (L_f + L_g))} = \frac{2V_{PN}K_{PWM}}{C_f L_f L_g}\left(\frac{1}{s(s^2 + 2\zeta\omega_{res}s + \omega_{res}^2)}\right) \quad (20)$$

where the damping constant K_{AD} is given by (21).

$$K_{AD} = \left(\zeta\, \omega_n\, L_f\right) \Big/ \left(V_{PN}\, K_{PWM}\right) \quad (21)$$

where z is the damping factor of the system and K_{PWM} is the PWM modulator gain.

SIMULATION AND EXPERIMENTAL VERIFICATIONS

The evaluation of the SS qZS-CMI operation, control structures and controllers is divided in steady-state and transient analysis.

In steady-state conditions, the key waveforms to describe the SS qZS-CMI operation as well as the quality of the controlled current injected to the grid are discussed. On the other hand, in the transient situation, the controller response to a step decrease of PV array irradiation is evaluated.

Simulation was performed to verify the theoretical analysis and confirm the proposed control method and topology. The proposed controller for the prototype SS qZS-CMI was built using the DSP-based universal digital-control board, which integrates interfaces for power supply, A/D conversion, serial communication, etc. Rewrite the system parameters in the experiment as follows: $L_{1(a)}$=$L_{1(b)}$=$L_{2(a)}$=$L_{2(b)}$= 2.568 mH, $C_{1(a)}$=$C_{1(b)}$=$C_{2(a)}$=$C_{2(b)}$= 4.7 mF, L_f= 1.750 mH, C_f= 4.242 uF, L_g= 0.860 mH, system output frequency f_g= 60 Hz, and switching frequency f_s= 10.02 kHz, and the total power of the system P_o= 1.5 kW.

STEADY-STATE OPERATION

Fig. 5(a) and 5(b) show the currents through the Main H-bridge and Auxiliary H-bridge, respectively. It can be seen in Fig. 5(a) that current $i_{L1(a)}$ ($\approx 9.5A$).

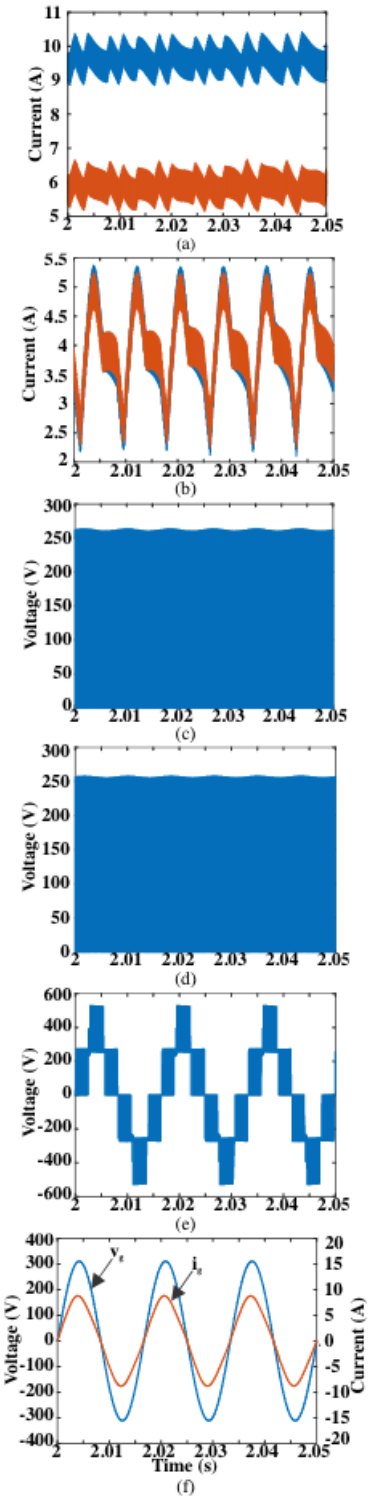


Fig. 5. Key waveforms. (a) Main H-bridge inductor currents $i_{L1(a)}$, $i_{L2(a)}$; (b) Auxiliary H-bridge inductor currents $i_{L1(b)}$, $i_{L2(b)}$; (c) Main H-bridge DC-bus voltage ($V_{PN(a)}$); (d) Auxiliary H-bridge DC-bus voltage ($V_{PN(b)}$); (e) Cascaded output voltage (Vo); (f) Grid current (i_g) and voltage (v_g).

is higher than $i_{L2(a)}$ (≈6A). The difference between then is the current through the auxiliary bridge multiplied by the coupled inductor turns ratio (N = 1.33), which is ≈ 4.65A. It also can be observed that besides the dc components, there are low frequencies components present in these waveforms.

Fig. 5(c) and 5(d) show that voltages $V_{PN(a)}$ and $V_{PN(b)}$ are approximately 255V, which ensures the symmetry between the main and auxiliary modules.

Fig. 5(e) shows the waveform at the output of the H-bridge modules before the LCL filter. It can be observed that this voltage is a five level-stepped PWM waveform. Each level is approximately 255V. Fig. 5(f) shows that the inverter provides a very high power factor by means of the analysis of the grid voltage (v_g) and current (i_g). Fig. 6 shows the frequency analysis of i_g. The frequency spectrum reveals that, besides fundamental frequency (60Hz), the third harmonic is also present (180Hz). The total harmonic distortion factor (THD) is about 5%. Decreasing the input power to 1.1 kW, around 75 % of nominal power, Fig. 7(a) show the injected current into the grid (i_g). Applying the method of current TDD, the results is 3.33%. Fig. 7(b) depicted the current injected into the grid with a PV power at the input of the converter below the nominal, around 0.75 kW (50% of nominal power) and the results of current TDD is 2.34%. Finally, at 0.5 kW (33 % of nominal power), in Fig. 7(c) is given the current injected into the grid According to the calculation method the current TDD is 1.42%. As can be seen, for all situation the current TDD attend the IEEE standard.

TRANSIENT OPERATION CONDITIONS

In order to evaluate the proposed control system, a test consisting in changing the PV voltage from 155 V to 105 V has been done.

Fig. 8(a) shows that at 2 s, the voltage step takes place. The MPPT control seeks for a novel maximum power point, which directly changes the shoot-through duty ratio of the main and the auxiliary H-bridges (Fig. 8(b)). On the other hand, the $V_{PN(a)}$ and $V_{PN(b)}$ controllers keep the dc bus voltage envelope at their reference values (Fig. 8(c)) and (8(d)). While the voltage and current of the photovoltaic array decrease, the grid current is decreasing from 6.81A to 4.62A (Fig. 8(e)). The power from each module also decreases from 660W to 420W (Fig. 8(f)). It is observed that the Phase-shift modulation is responsible to distribute the power equally among the cascaded H-bridge modules.

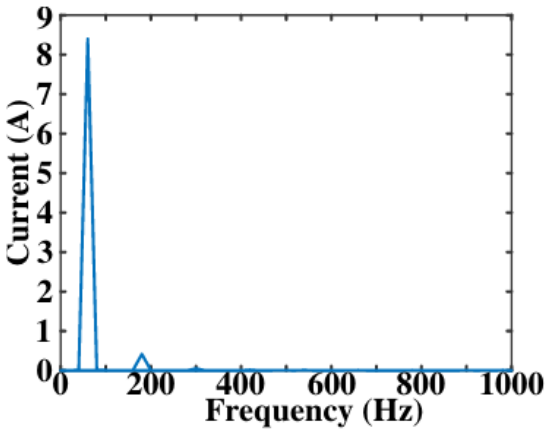
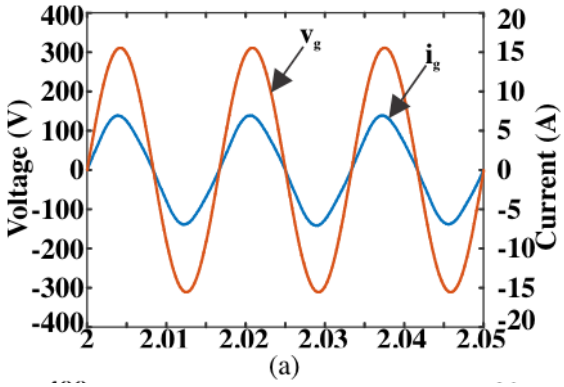


Fig. 6. Harmonic spectrum of the grid current (i_g).



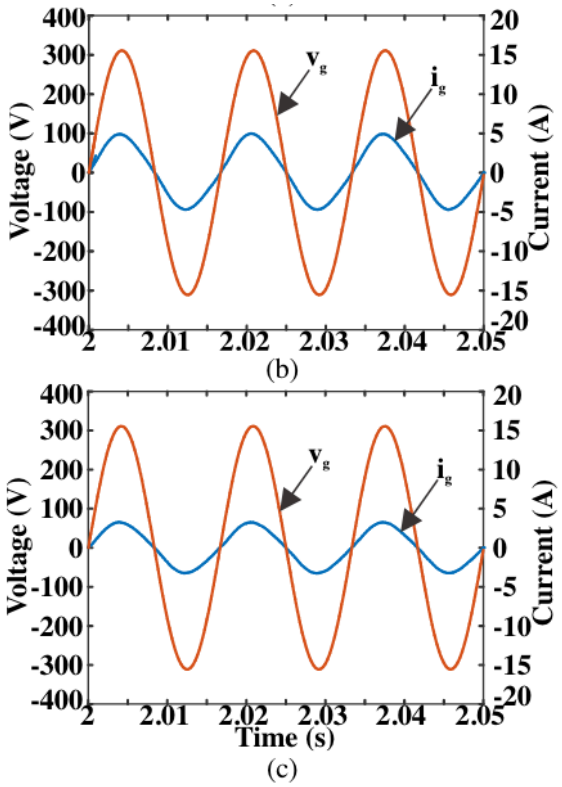


Fig. 7. Simulation results waveforms. (a) Grid current (i_g) and voltage (v_g) for a power of 1.1 kW; (b) Grid current (i_g) and voltage (vg) for a power of 0.75kW;(c) Grid cur-rent (i_g) and voltage (v_g) for a power of 0.5kW.

CONCLUSIONS

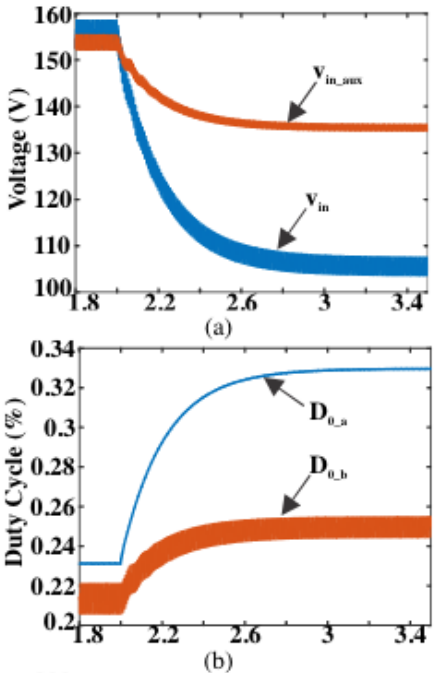
This paper has presented a novel cascade multilevel qZ-Source inverter topology. Compared to other qZ-Source inverters, the named SS qZS-CMI has the ability to make use of a single dc source to provide active power to all cascaded qZ-Source modules. It is accomplished by replacing its Z-impedance inductances by coupled inductors. Each secondary winding of a coupled inductor provides power to the input capacitor of an auxiliary module through a rectifier diode operating as a forward converter. This way, active power can be shared among the cascaded modules enabling all benefits of power sharing such as the modules derating and better heat management by means of the losses distribution. Additionally, a control

method for SS qZS-CMI based single-phase grid-tie PV system is proposed.

The grid-injected power was fulfilled at unity power factor, only the main SS qZS-HBI modules achieved the maximum power points tracking. Moreover, the independent dc-link voltage closed-loop control ensured all SS qZS-HBI modules have the voltage balance, which provides accurate symmetry to the output voltage levels, enhancing the quality for the grid current waveform without large grid filters. The control parameters were well designed to ensure system stability and fast response.

The control system of the proposed topology includes MPPT control to the PV array, independent dc-link voltage control for each cascaded qZS module, active damping for the LCL grid filter, and very good transient and steady state response through a P+resonant grid current dual-loop control strategy.

A 1.5 kW simulation model is built to test the performance of the system. Simulation results verify the operating principle and control strategies of the proposed system.



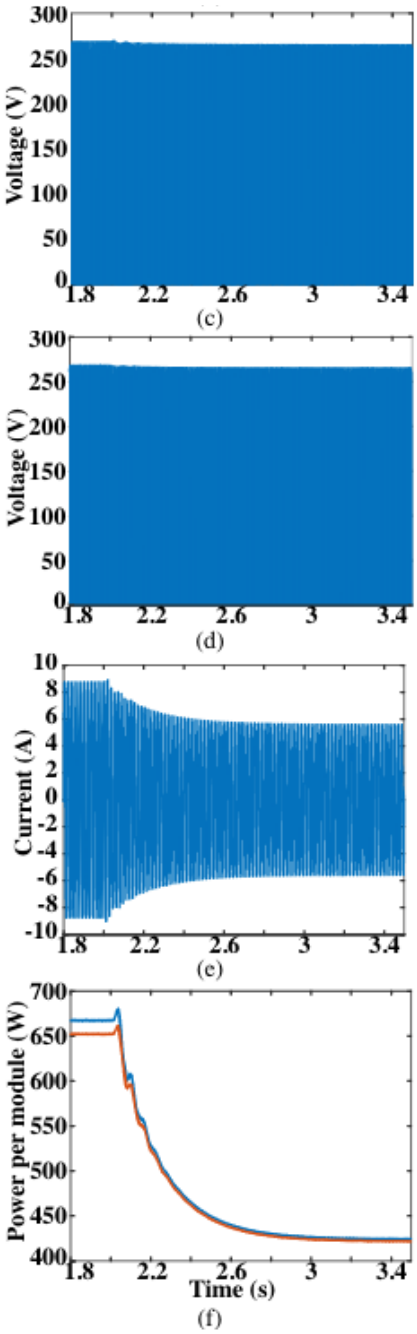


Fig. 8. Key waveforms. (a) Input voltage (V_{in}); (b) Shoot-through duty ratio ($D_{0(a)}$) ($D_{0(b)}$); (c) Main H-bridge DC-bus voltage ($V_{PN(a)}$) (d) Auxiliary H-bridge DC-bus voltage ($V_{PN(b)}$); (e) Grid current (i_g); (f) Power behavior in each module.

ACKNOWLEDGMENT

This paper was supported by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior (PROEX/CAPES).

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